UNIVERSIDADE FEDERAL DE SANTA CATARINA
PROGRAMA DE PÓS-GRADUAÇÃO EM ENGENHARIA ELÉTRICA

Andrés Fernando Ordóñez Hurtado

DESIGN METHODOLOGY OF A MODULAR CMOS ULTRA-LOW POWER SELF-BIASED CURRENT SOURCE

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Orientador: Prof. Dr. Carlos Galup-Montoro

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Esta Dissertação foi julgada aprovada para a obtenção do Título de "Mestre", e aprovada em sua forma final pelo Programa de Pós-Graduação em Engenharia Elétrica.

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Este trabajo está dedicado a mi madre María del Socorro y a mis hermanos Rodrigo Hernán y Eduardo José.

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ABSTRACT

In this document a design procedure of a CMOS ultra-low-power self-biased current source is developed. A modular topology using two self-cascode MOSFETs (SCMs), a current mirror and an operational amplifier is implemented. The described methodology is based on the concept of inversion level, and the design space of the current source is described mainly in terms of the specifications of the operational amplifier and the PMOS current mirror. The circuit was designed in a 130 nm standard CMOS technology. Simulation results are provided to validate the design methodology and the performance of the current source, showing that the proposed circuit can operate at a supply voltage less than 1 V with less than 1%/V of line regulation.

Keywords: CMOS. Self-biased current source, Self-cascode MOSFET. Design methodology. Inversion level.

RESUMO

Neste documento é desenvolvida uma metodologia de projeto de uma fonte de corrente auto polarizada de ultra baixo consumo de potência em tecnologia CMOS. É descrita uma topologia modular implementada com dois MOSFETs auto cascodados (SCMs) e um amplificador operacional. A metodologia proposta está baseada no conceito de níveis de inversão e o espaço de projeto do circuito é descrito principalmente em termos das especificações do amplificador operacional e do espelho de corrente PMOS. O circuito foi projetado usando uma tecnologia padrão CMOS de 130 nm. Os resultados das simulações são apresentados neste documento para validar a metodologia de projeto e o desempenho da fonte de corrente, mostrando que o circuito proposto pode operar com uma tensão de alimentação menor de 1 V e com menos de 1%/V na regulação de linha.

Palavras-chave: CMOS. Fonte de corrente auto polarizada, MOSFET auto cascodado. Metodologia de projeto. Nível de inversão.

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LIST OF ABBREVIATIONS

AC	Alternate Current
ACM	Advanced Compact MOSFET
CMOS	Complementary Metal Oxide Semiconductor
CTAT	Complementary-to-Absolute Temperature
DC	Direct Current
KVL	Kirchoff Voltage Law
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	n-type Metal Oxide Semiconductor
ORA	Operational Transresistance Amplifier
OTA	Operational Transconductance Amplifier
PMOS	p-type Metal Oxide Semiconductor
PSRR	Power Supply Rejection Ratio
PTAT	Proportional-to-Absolute Temperature
SCM	Self-cascode MOSFET
TC	Temperature Coefficient
UCCM	Unified Charge-Control Model
UICM	Unified Current-Control Model
VFCM	Voltage-Following Current Mirror

LIST OF SYMBOLS

A	Transistor area
C_L	Load capacitance
C'_{ox}	Oxide capacitance per unit area
f_u	Unity-gain frequency
g_m	Gate transconductance
I_D	Drain Current
i_f	Forward inversion level
I_F	Forward current
i_r	Reverse inversion level
I_R	Reverse current
I_{REF}	Reference current
I_{SQ}	Normalized specific current
k	Boltzmann constant
K_{MI}	Moderate inversion coefficient
K_{WI}	Weak inversion coefficient
L	Transistor channel length
L_{EQ}	Equivalent transistor channel length
L_U	Unity transistor channel length
n	Slope factor
q	Electron charge
q'_{ID}	Normalized charge density at drain
q'_{IS}	Normalized charge density at source
S	Aspect ratio
T	Temperature
U_{OS}	Normalized input offset voltage
U_{REF}	Normalized reference voltage
V_D	Drain voltage
V_{DD}	Supply voltage
V_{DS}	Drain-to-source voltage
V_{ER}	Error voltage
V_G	Gate voltage
V_{OS}	Input offset voltage

V_P	Pinch-off voltage
V_{REF}	Reference voltage
V_S	Source voltage
V_{T0}	Zero-bias threshold voltage
W	Transistor channel width
W_{EQ}	Equivalent transistor channel width
W_U	Unity transistor channel width
α	Geometric ratio
ΔI_D	Current mismatch
Δi_f	Error in inversion level
ΔV_{REF}	Error in reference voltage
ε_{I_D}	Normalized current mismatch
ε_{i_f}	Normalized error in inversion level
μ	Carrier mobility
ϕ_t	Thermal voltage

CONTENTS

1 INTRODUCTION

In analog circuit design, one of the fundamental requirements is to bias all the blocks and sub-blocks in the appropriate operating point. In most of the analog circuits, including oscillators, bandgap references, D/A converters and sensors [1–4], biasing is provided by a circuit capable of generating a stable reference current, defined in terms of physical parameters such as the thermal voltage or the carrier mobility. To this end, it is necessary that all the components of the circuit are included in the silicon chip. For energy harvesting circuits or implantable devices, the usage of discrete external components it is not feasible due to the increased production cost and the larger size of the final devices, in addition to the requirement of using extra pins on the chip (which increases the silicon area). On the other hand, in ultra-low-power systems it is essential to minimize the quiescent current of all the sub-blocks in order to maximize the lifetime of batteries (if they were used).

To reduce the high power consumption in Complementary Metal Oxide Semiconductor (CMOS) technologies, various current sources based on sub-threshold operation of the MOSFET have been proposed. Some of them include resistors [5], transistors operating in linear region [6] or series association of transistors [7, 8]. In the following section, the most relevant circuits that generate a current reference in standard CMOS technologies, along with some techniques to overcome possible drawbacks, are summarized. Finally, the motivation and the objective of this master dissertation is presented, taking into account the advantages and limitations of the current references to be described next.

1.1 BIBLIOGRAPHIC REVIEW

In CMOS technologies, many current sources have been designed. One of the most referenced is the classical, supply-independent self-biased current source composed of two current mirrors connected in a positive feedback loop shown in Fig. 1 [5]. N_1 and N_2, with a proportionality factor $K = S_2/S_1$, operate in weak inversion to generate a Proportional-to-Absolute Temperature (PTAT) voltage which is converted to current through the resistor R.

By applying Kirchoff's Voltage Law (KVL) to the loop formed

by N_1, N_2 and R, the reference current is given by

$$I_{REF} = \phi_t \frac{\ln(K)}{R}, \tag{1.1}$$

where $\phi_t = kT/q$ is the thermal voltage, k is the Boltzmann constant, T is the absolute temperature, and q is the electron charge. Commonly a start-up circuit is required to force the circuit to drive a transient current until the stable equilibrium state is reached. After that, the gain of the positive feedback loop is reduced and the current converges to the desired value.

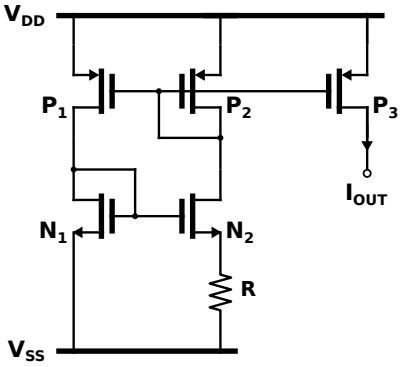


Figure 1: Self-biased current source with resistor [5].

One of the drawbacks of this current source is the use of a high resistance to reduce the quiescent current, which demands a considerable amount of silicon area. Process variability of the resistors available in CMOS technologies of approximately 10% and 20% [9] also has a negative influence in the robustness of the current source. In [10], a technique to improve the power supply rejection is presented where a NMOS cross-coupled pair is included in this circuit.

To solve the area trade-off originated by the use of an integrated resistor, some current sources have been designed using transistors operating in the linear region to replace the passive components. One of these circuits is presented in Fig. 2, where N_4 is operating in strong inversion, linear region and N_3 in strong inversion, saturation region to generate the gate bias voltage of the NMOS resistor [6].

The adequate sizing of the transistors allows the output current to be proportional to the specific current of the transistor, a parameter which has a very small variation with temperature. In [11], the output

current of the circuit in Fig. 2 has been deduced, yielding

$$I_{REF} = 2n\mu_n C'_{ox}\phi_t^2 S_4 A \ln^2(K), \tag{1.2}$$

where n is the slope factor, μ_n is the carrier mobility in NMOS transistor, C'_{ox} is the oxide capacitance per unit area, $A = S_4/S_3$, and $K = S_1/S_2$. The authors of [11] use the EKV MOSFET model, in which the specific current of the NMOS transistor is defined as $I_{SQ} = 2n\mu_n C'_{ox}\phi_t^2$ [12]. Thus, it is clear from (1.2) that I_{REF} is proportional to I_{SQ}.

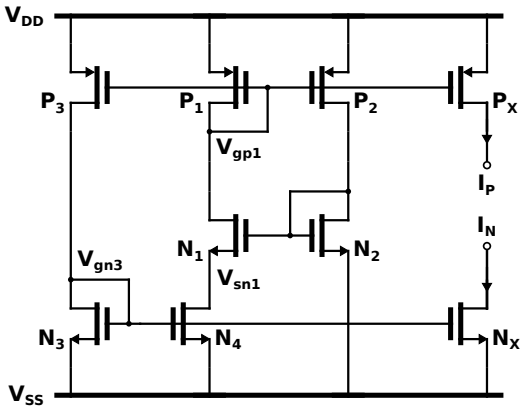


Figure 2: Self-biased current source without resistor [6].

The self-cascode MOSFET (SCM) structure is another alternative to replace the resistors in current sources. This structure consists of a series association of two transistors operating in the linear and saturation regions, respectively. The current source proposed in [7] and also reported in [13] (shown in Fig. 3) consists of two SCMs, operating in weak (M_{1A} and M_{1B}) and strong inversion (M_{5A} and M_{5B}), respectively; both SCMs are biased to have equal intermediate voltages (V_{CH1} and V_{CH5}) but different inversion coefficients, obtained with the adequate PMOS proportionality factors. The intermediate branch formed by M_3 and M_7 is used to balance both V_{CH1} and V_{CH5}. The stable equilibrium state of the current source is reached when these voltages are equal. Both SCMs are formed by the series and parallel association of unity transistors to reduce the threshold voltage mismatch (the authors suggest to increase the intermediate voltage to reduce these mismatch). As in [6], the output current of the circuit in Fig. 3 is proportional to the specific current of the NMOS transistor. Despite

that the circuit can operate at low supply voltage, this structure is not appropriate for ultra-low-power applications because M_5 is biased at a current $N\dot{M}$ times higher than M_1.

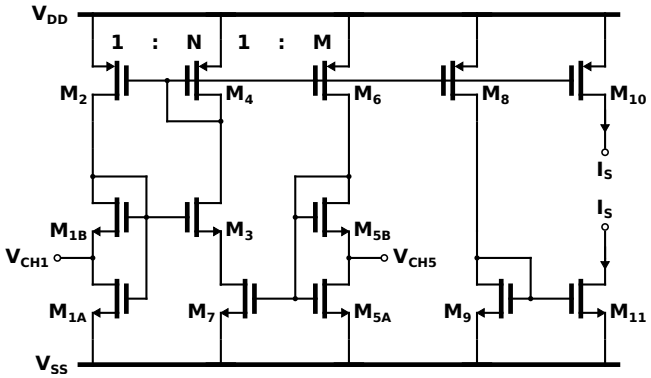


Figure 3: Specific current extractor [7].

Another current source that uses SCMs is described in [14], here shown in Fig. 4. The concept of this circuit is similar to the one presented in [5], with the difference that the gate voltage in the NMOS transistor is increased by using multiple stacked SCMs operating in weak inversion as described in [15]. The PTAT voltage generated across the drain-to-source voltage of M_2, M_4, M_6, M_8, and M_{10} is enough to bias M_1 in strong inversion.

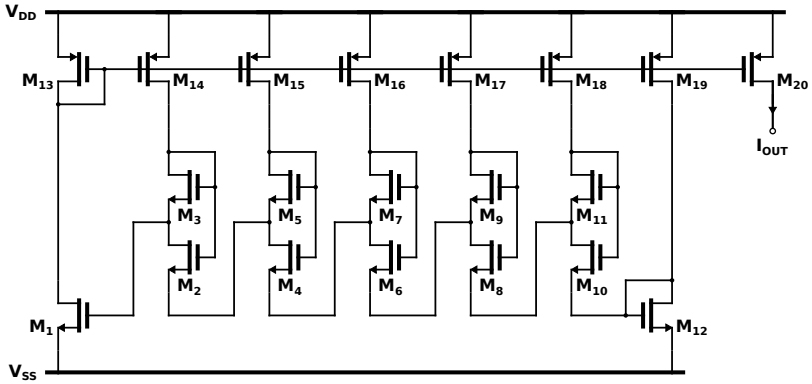


Figure 4: Temperature-compensated current reference [14].

As in [7], the influence of the threshold variation is reduced using series and parallel association of unity transistors for all the SCM transistors. The power dissipation of this circuit is high due to the additional current branches needed to bias all the SCMs.

The current source shown in Fig. 5 [8] is a self-biased specific current generator that uses two SCMs biased in weak and moderate inversion, coupled by a Voltage-Following Current Mirror (VFCM) composed of M_6 - M_9. This circuit is able to operate at low voltages, exhibiting low sensitivity to the supply voltage. In this circuit, the node voltage $V_{X(WI)}$ can be either zero or a PTAT voltage generated through a second SCM operating in weak inversion (M_3 and M_4). Due to the metastable nature of this current source, a start-up block is required to bias the circuit in the stable operating point.

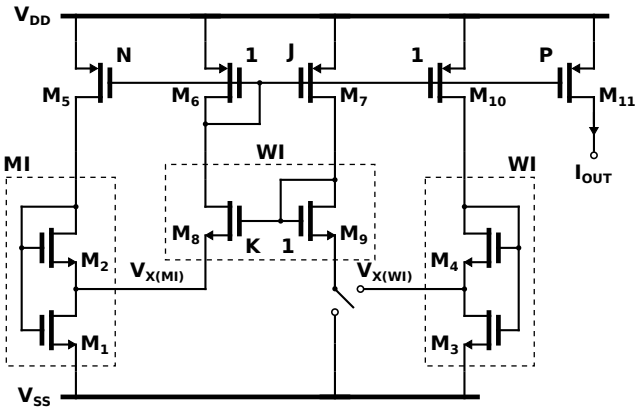


Figure 5: Self-biased current source [8].

For the first time in [8] the current source design was done in all the regimes of the MOS transistor, including weak and moderate inversion, excluding strong inversion, using the Advanced Compact MOSFET (ACM) model [16, 17] which introduces a reduced number of equations to represent adequately the behavior of the transistor in terms of the inversion level in all the operation regions.

In [18], the circuit shown in Fig. 6 is proposed. In this case, one SCM operating in strong inversion is used, and the operational trans-resistance amplifier (ORA) formed by M_3 - M_8 replaces the single PMOS current mirror. A PTAT voltage across M_{11} is generated by M_1 and M_2, which operate in weak inversion.

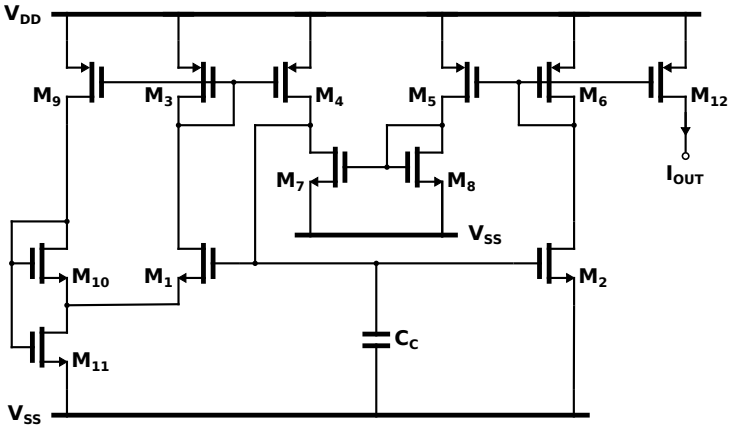


Figure 6: Self-biased current source [18].

The feedback of this structure improves the Power Supply Rejection Ratio (PSRR) of the circuit. A compensation capacitor C_C needs to be incorporated to maintain the stability of the circuit, increasing the required silicon area. The temperature compensated current reference circuit proposed in [19] has a structure based on the circuit of Fig. 6, including two modified SCMs with additional branches connecting the base of bipolar transistors to adjust the temperature behavior of the output current.

Some modern current sources have been designed using a variety of techniques. In [20], the ultra-low power current reference shown in Fig. 7, which is of low sensitivity to both temperature and supply voltage is presented. All transistors operate in weak inversion, except for M_3, which operates in strong inversion in the linear region, and M_4 in strong inversion in saturation region. In this circuit, a start-up circuit is required to avoid the stable state in the zero-bias condition. PMOS cascode current mirrors are used to improve the power supply rejection, but at the expense of increasing the minimum supply voltage.

Finally, in [21] an all-MOS current reference circuit is presented. The structure is based on the circuit described in [6], and it is very similar to the circuit shown in Fig. 7, except for a branch that was removed to reduce power consumption. The circuit equalizes the thermal slopes of the gate voltage and the threshold voltage of the NMOS, reducing the temperature coefficient of the output current at the cost of an increase in the power consumption. Cascode devices were also used to improve the PSRR performance.

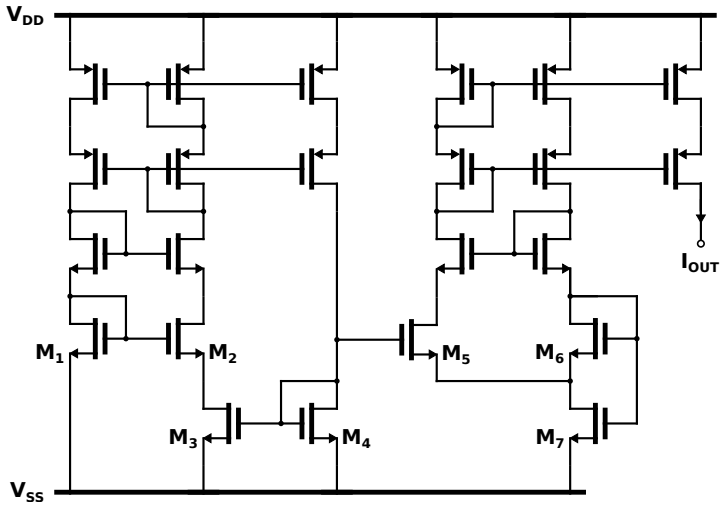


Figure 7: Self-biased current source [20].

Table 1 summarizes the main characteristics of the CMOS reference current sources found in literature, including technological process, minimum supply voltage, power consumption, among others.

1.2 MOTIVATION

As seen in the previous section, most of the current reference circuits found in the literature use CMOS transistors operating in different regions. The SCM is a good option to generate a stable PTAT low voltage to replace the passive components. Using two SCMs, as shown in [8], increases the symmetry and the immunity to mismatch variations. Despite the fact that the VFCM offers some advantages when the transistors operate in weak inversion, the voltage transfer is not precise enough and the circuit can be susceptible to current deviations. In other references [5–7, 14], when two SCMs structures were used, the operation regions of them were reduced only to weak and strong inversion, and the design space of the intermediate inversion levels has not been explored. If using a modular topology, the complete design space can be expressed in terms of the specifications of the sub-blocks of the circuit.

1.3 OBJECTIVE

The main objective of this master dissertation is to develop a design methodology and procedure of a modular CMOS SCM-based self-biased current source in terms of the specifications of the sub-blocks (operational amplifier, current mirror) to describe the complete design space of such a current source. The analysis is made using the equations of the ACM model, including the errors associated to the basic components that forms the circuit: i) a unity gain current mirror, and ii) an operational amplifier.

1.4 ORGANIZATION

This dissertation is organized as follows. In Chapter 2, the design procedure of the current source in terms of the specifications of the sub-blocks (operational amplifier, current mirror) is described. In Chapter 3, the design of the sub-blocks of the self-biased current source is presented. In Chapter 4, the schematic and post-layout simulation results of the designed circuits are presented. Finally, the conclusions and suggestions for further work are presented in Chapter 5.

Table 1: Comparison of Reported Self-Biased Current Reference Circuits

Parameter	[6]	[8]	[14]	[18]	[19]	[20]	[21]
Process	2 μm	1.5 μm	3 μm	1.2 μm	0.25 μm	0.35 μm	0.18 μm
I_{OUT}	6 nA	0.4 nA	774 nA	320 nA	45 nA	100 nA	92.2 nA
Min V_{DD}	1.2 V	1.1 V	3.5 V	0.9 V	1.2 V	1.8 V	1.25 V
Power	7.2 nW	2 nW	10 μW	2.5 μW	-	1 μW	0.67 μW
Line Reg.	10%/V	6%/V	150 ppm/V	-	0.318%/V	0.2%/V	7.5%/V
TC	-	0.3%/°C	0.04%/°C	1.15 nA/°C	0.026%/°C	600ppm/°C	177ppm/°C
Area	0.06 mm^2	0.045 mm^2	0.2 mm^2	0.05 mm^2	0.25 mm^2	0.015 mm^2	0.0013 mm^2
Features	NMOS as resistor	SCM in WI and MI	Stacked SCM	One SCM and ORA	Two SCM and ORA	SCM and NMOS as resistor	SCM and NMOS as resistor

2 DESIGN METHODOLOGY OF A CMOS SELF-BIASED CURRENT SOURCE

In order to develop a design methodology for the modular self-biased current source, a model that correctly describes the behavior of the MOS transistor in all regions of operation is required. Initially, in this chapter, the ACM model will be briefly described; after that, the design methodology of the self-biased current source will be introduced.

2.1 THE ADVANCED COMPACT MOSFET (ACM) MODEL

The ACM model gives the drain current of the MOSFET transistor (I_D) in terms of the forward (I_F) and reverse (I_R) components in all the operating regions [16] as

$$I_D = I_F - I_R = I_{SQ}\ S\ \left(i_f - i_r\right), \tag{2.1}$$

where $S = \frac{W}{L}$ is the aspect ratio of the transistor, W is the channel width, L is the channel length, i_f and i_r are the forward and reverse inversion levels, respectively, and I_{SQ} is the normalized specific current given by

$$I_{SQ} = \frac{1}{2}\mu C'_{ox} n \phi_t^2. \tag{2.2}$$

Expressing the inversion levels in terms of the normalized inversion charge densities results in

$$i_{f(r)} = \left[q'_{IS(D)} + 1\right]^2 - 1, \tag{2.3}$$

where q'_{IS} and q'_{ID} are the normalized inversion charge densities at source and drain, respectively. Replacing (2.3) in (2.1) yields

$$I_D = I_{SQ}\ S\ \left[(q'_{IS}+1)^2 - (q'_{ID}+1)^2\right]. \tag{2.4}$$

The relation between the normalized charge densities and the voltages, called the Unified Charge-Control Model (UCCM), is given in [16] as

$$\frac{V_P - V_{S(D)}}{\phi_t} = q'_{IS(D)} - 1 + \ln\left[q'_{IS(D)}\right], \tag{2.5}$$

where V_S and V_D are the source-to-bulk and drain-to-bulk voltages, and

V_P is the pinch-off voltage defined as

$$V_P \approx \frac{V_G - V_{T0}}{n}, \tag{2.6}$$

with V_G being the gate-to-bulk voltage and V_{T0} the zero-bias threshold voltage.

The relation between the normalized currents and the voltages, called the Unified Current-Control Model (UCCM) obtained from (2.3) and (2.5) is

$$\frac{V_P - V_{S(D)}}{\phi_t} = F\left[i_{f(r)}\right] = \sqrt{1 + i_{f(r)}} - 2 + \ln\left[\sqrt{1 + i_{f(r)}} - 1\right]. \tag{2.7}$$

From (2.5) is clear that the drain-to-source voltage V_{DS} of the transistor in all the operation regions is given by

$$\frac{V_{DS}}{\phi_t} = q'_{IS} - q'_{ID} + \ln\left(\frac{q'_{IS}}{q'_{ID}}\right), \tag{2.8}$$

or using (2.7) becomes

$$\frac{V_{DS}}{\phi_t} = \sqrt{1 + i_f} - \sqrt{1 + i_r} + \ln\left(\frac{\sqrt{1 + i_f} - 1}{\sqrt{1 + i_r} - 1}\right). \tag{2.9}$$

More details about the ACM model can be found in [16, 17].

2.2 SELF-CASCODE MOSFET (SCM)

As seen in Section 1.1, the SCM is the core of several self-biased current sources, commonly used as a PTAT low voltage generator. In the SCM of Fig. 8, M_1 is in triode region and M_2 is in saturation region. The current flowing through each transistor is

$$I_{D1} = I_{SQ}\ S_1\ \left(i_{f_1} - i_{r_1}\right) = I_D, \tag{2.10}$$

$$I_{D2} \approx I_{SQ}\ S_2\ i_{f_2} = I_D. \tag{2.11}$$

Since $V_{D1} = V_{S2}$, then $i_{r_1} = i_{f_2}$. The equalization of the two currents results in

$$i_{f_1} = \left(1 + \frac{S_2}{S_1}\right) i_{f_2} = \alpha_1\ i_{f_2}. \tag{2.12}$$

Applying UICM to both transistors, and since $V_{P1} = V_{P2}$, the intermediate voltage is

$$V_{REF} = \phi_t \left[F(i_{f_1}) - F(i_{f_2}) \right] = \phi_t \left[F(\alpha_1 \; i_{f_2}) - F(i_{f_2}) \right]. \tag{2.13}$$

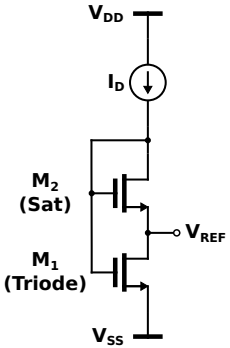


Figure 8: Self-cascode MOSFET.

Using (2.7) and (2.13), the first-order approximation of V_{REF} for $\alpha_1 \; i_{f_2} << 1$ is

$$V_{REF} \approx \phi_t \left[\ln(\alpha_1) + \frac{\alpha_1 - 1}{4} i_{f_2} \right]. \tag{2.14}$$

If M_2 operates deep in weak inversion ($i_{f_2} \to 0$), then (2.14) reduces to

$$V_{REF} \to \phi_t \ln(\alpha_1), \tag{2.15}$$

which is a PTAT voltage with a slope dependent on the ratio of the aspect ratios of the SCM transistors only.

2.3 CURRENT SOURCE DESIGN

The proposed current source in this master dissertation, shown in Fig. 9, is based on the circuits presented in [7] and [8], with the main difference that the VFCM is replaced by an ultra-low-power operational amplifier to couple the intermediate voltages of the SCMs. The bulk of all NMOS transistors are tied to the ground potential (V_{SS}), while the bulf of all PMOS transistors are tied to the voltage supply potential (V_{DD}).

The concept of self-biasing of this circuit consist in mirroring the output current to bias the operational amplifier connected in closed loop [22] in order to force the intermediate voltages of both SCMs to be the same. The SCM composed of M_1 and M_2 ideally operates deep in weak inversion and generates a PTAT reference voltage V_{REF}. The error voltage source V_{ER} connected to the inverting input of the operational amplifier represents the sum of the input offset voltage (V_{OS}) and the contribution of the threshold voltage mismatch of the SCM transistors. If $V_{ER} = 0$, it follows from (2.13) and (2.15) that

$$\ln(\alpha_1) = F(\alpha_3\ i_{f4}) - F(i_{f4}), \tag{2.16}$$

where $\alpha_1 = 1 + \frac{S_2}{S_1}$ and $\alpha_3 = 1 + \frac{S_4}{S_3}$. Thus, the inversion level of M_4 is constant and depends only on the geometric ratios α_1 and α_3, and the output reference current $I_D = I_{SQ}\ S_4\ i_{f_4}$ is proportional to the specific current of M_4.

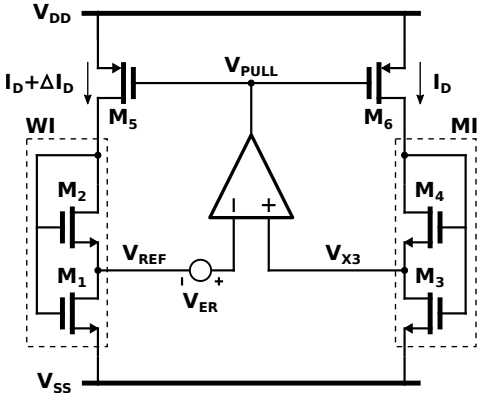


Figure 9: Modular self-biased current source.

The operating point of the current source depends on the values of α_1 and α_3, as shown in Fig. 10. For $\alpha_1 << \alpha_3$, M_3 and M_4 operate at the high end of moderate inversion and the intersection of the two V_X (I_D) is very precise. On the other hand, if $\alpha_1 \approx \alpha_3$, the two curves are close to each other, and the operating point is very sensitive to the errors in the device parameter. Thus, to make the appropriate choice of the moderate inversion level, it is important to assess the effect of the circuit and device parameters errors on the operating point of the current source.

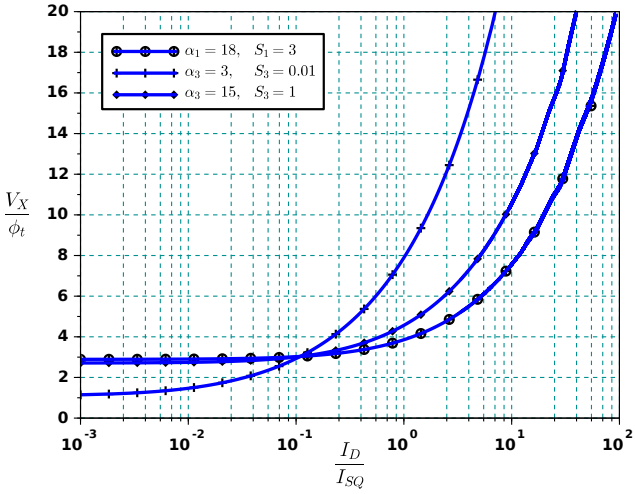


Figure 10: Operating point for different values of α.

2.3.1 Error Analysis

The current source in Fig. 9 is susceptible to variations caused by mismatches in both the operational amplifier and the current mirror. The effect of the input offset voltage on the inversion level of M_4 is

$$\frac{\Delta i_{f_4}}{i_{f_4}} = \frac{V_{OS}}{\phi_t} \frac{2}{\sqrt{1+\alpha_3\, i_{f_4}} - \sqrt{1+i_{f_4}}}, \tag{2.17}$$

as calculated in Appendix A. From (2.17), it is clear that, independently of the input offset voltage, if M_4 operates deep in strong inversion (i.e. $i_{f_4} >> 1$) then the error in i_{f_4} is negligible. Strong inversion operation is not appropriate in ultra-low-power circuits; therefore, it is important to explore the design space of the circuit in terms of the mismatch of the current mirror ($\Delta I_D/I_D$) and the value of V_{OS}.

The normalized errors are

$$U_{OS} = \frac{V_{OS}}{\phi_t}, \tag{2.18}$$

$$\varepsilon_{i_{f_4}} = \frac{1}{2}\frac{\Delta i_{f_4}}{i_{f_4}}. \tag{2.19}$$

Replacing (2.3) in (2.17) and isolating the terms related to the

normalized inversion charges gives

$$K_{MI} = \frac{U_{OS}}{\varepsilon_{i_{f_4}}} = q'_{IS_3} - q'_{ID_3}. \tag{2.20}$$

Thus, from (2.8), (2.16) and (2.20), the normalized inversion charge densities of M_3 can be calculated as

$$q'_{IS_3} \approx K_{MI} \frac{e^{U_{REF}-K_{MI}}}{(e^{U_{REF}-K_{MI}})-1}, \tag{2.21}$$

$$q'_{ID_3} \approx K_{MI} \frac{1}{(e^{U_{REF}-K_{MI}})-1}, \tag{2.22}$$

where $U_{REF} = \frac{V_{REF}}{\phi_t}$. The result is a set of possible solutions for aspect ratios and inversion levels of the two SCMs transistors, as follows

$$i_{f_4} = (1 + q'_{ID_3})^2 - 1, \tag{2.23}$$

$$\alpha_3 = \frac{(1 + q'_{IS_3})^2 - 1}{(1 + q'_{ID_3})^2 - 1}, \tag{2.24}$$

and the transistors aspect ratios are given by

$$S_4 = \frac{I_D}{I_{SQ}\ i_{f_4}}, \qquad S_3 = \frac{S_4}{\alpha_3 - 1}. \tag{2.25}$$

By analyzing (2.21) and (2.22), it is clear that the design space is in the interval $U_{REF} > K_{MI} > 0$. The asymptotic cases of (2.21) - (2.25) are:

- If $K_{MI} \to U_{REF}$, then $q'_{IS_3} \approx q'_{ID_3} \to \infty$. In this case, M_3 operates deep in strong inversion in the linear region, $\alpha_3 \to 1$, and the ratio $\frac{S_4}{S_3}$ tends to zero.
- If $K_{MI} \to 0$, then both q'_{IS_3} and q'_{ID_3} tend to zero, M_4 operates deep in weak inversion, and thus

$$\alpha_3 = \frac{q'_{IS_3}}{q'_{ID_3}} \approx e^{U_{REF}} \approx \alpha_1, \tag{2.26}$$

Based on the above considerations, it is clear that the design interval for the SCMs is

$$1 < \alpha_3 < \alpha_1. \tag{2.27}$$

The results for (2.23) and (2.24) are those presented in Fig. 11 and Fig. 12, respectively, for five different values of K_{MI}, where $5\% < \Delta i_{f_4}/i_{f_4} < 65\%$ and 1 mV $< V_{OS} <$ 5 mV. The arrow indicates the effect of increasing the value of K_{MI}.

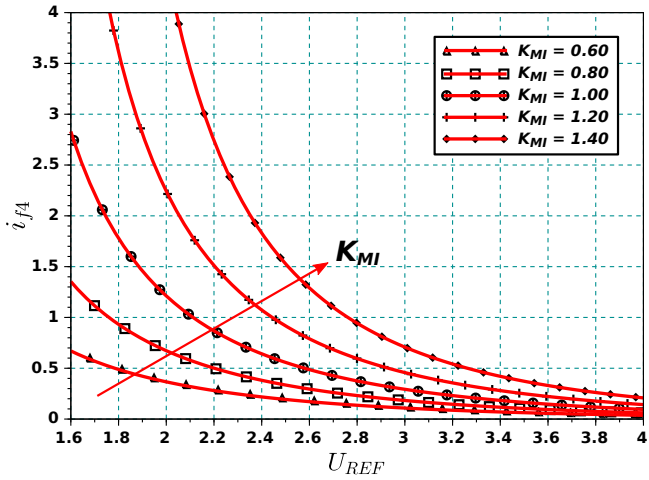


Figure 11: i_{f_4} vs. U_{REF}, for different values of K_{MI}.

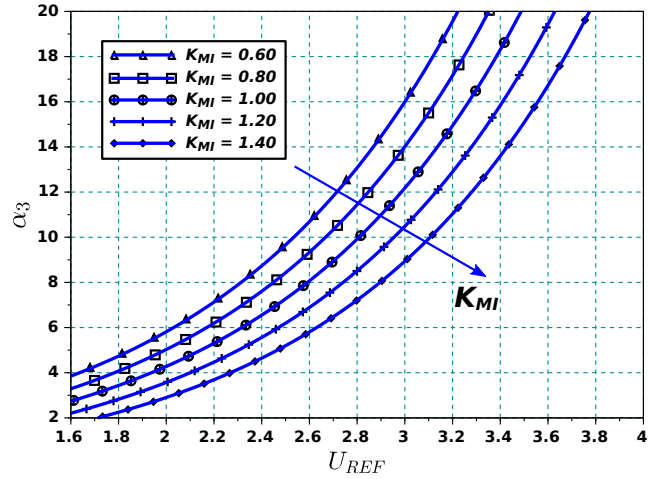


Figure 12: α_3 vs. U_{REF}, for different values of K_{MI}.

Replacing $U_{REF} = \ln(\alpha_1)$ in, Fig. 12 can be replotted, to obtain α_3 in terms of α_1, as shown in Fig. 13, where it is observed that $\alpha_3 < \alpha_1$.

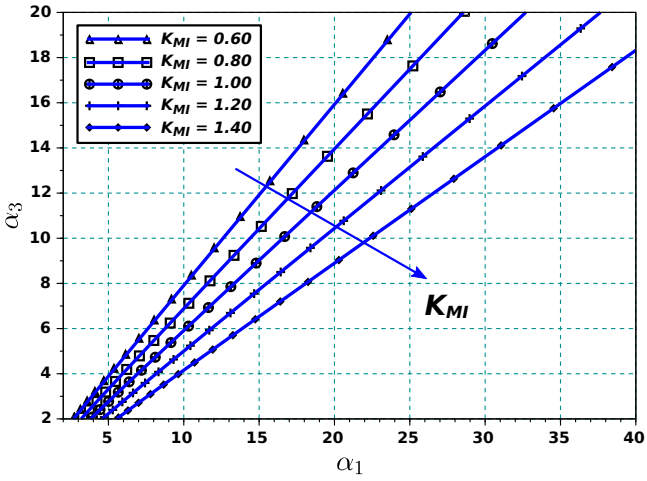


Figure 13: α_3 vs. α_1, for different values of K_{MI}.

In Table 2, possible combinations of the specification to produce the K_{MI} values used in Fig. 12 and 13 are presented.

Table 2: $\Delta i_{f_4}/i_{f_4}$ as function of V_{OS} and K_{MI}.

V_{OS} \ K_{MI}	**0.60**	**0.80**	**1.0**	**1.20**	**1.40**
1 mV	12.87 %	9.65 %	7.72 %	6.43 %	5.51 %
2 mV	25.74 %	19.31 %	15.44 %	12.87 %	11.02 %
3 mV	38.61 %	28.96 %	23.17 %	19.31 %	16.53 %
4 mV	51.48 %	38.61 %	30.89 %	25.74 %	22.04 %
5 mV	64.35 %	48.26 %	38.61 %	32.17 %	27.54 %

On the other hand, assuming that M_2 operates in weak inversion, the normalized intermediate voltage U_{REF} can be approximated using

(2.14) as

$$U_{REF} = \ln(\alpha_1) + \left(\frac{\alpha_1 - 1}{4}\right) \frac{I_D + \Delta I_D}{I_{SQ}\ S_2}. \tag{2.28}$$

The above expression can be split into two parts:

- The normalized reference voltage U_{REF} generated by the weak inversion SCM:

$$U_{REF} = \ln(\alpha_1) + \left(\frac{\alpha_1 - 1}{4}\right) i_{f_2}. \tag{2.29}$$

- The error in the reference voltage produced by the current mirror error is

$$\frac{\Delta V_{REF}}{\phi_t} = \frac{\Delta I_D}{I_D} \left(\frac{\alpha_1 - 1}{4}\right) i_{f2}. \tag{2.30}$$

The normalized errors are

$$\Delta U_{REF} = \frac{\Delta V_{REF}}{\phi_t}, \tag{2.31}$$

$$\varepsilon_{I_D} = \frac{1}{2} \frac{\Delta I_D}{I_D}. \tag{2.32}$$

Combining (2.30)-(2.32) gives

$$K_{WI} = \frac{\Delta U_{REF}}{\varepsilon_{I_D}} = \left(\frac{\alpha_1 - 1}{2}\right) i_{f_2} = \frac{1}{2}\ \frac{S_2}{S_1}\ i_{f_2}, \tag{2.33}$$

and the transistors aspect ratios can be calculated as

$$S_2 = \frac{I_D}{I_{SQ}\ i_{f_2}}, \qquad S_1 = \frac{S_2}{\alpha_1 - 1}. \tag{2.34}$$

For values of i_{f_2} below 0.1, the linear approximation (2.28) is adequate. For larger values, the complete -all regions- expression (2.13) should be used.

The results for (2.29) and (2.30) are those presented in Fig. 14 and Fig. 15, respectively, for five different values of K_{WI}, where 5 μV $< \Delta V_{REF} <$ 2mV and 4 % $< \Delta I_D/I_D <$ 20 %. The arrow indicates the effect of increasing the value of K_{WI}.

Selecting a common U_{REF} in Fig. 11, 12 and 14 generates a solution for each SCM: ($\alpha_1,\ i_{f_2}$) and ($\alpha_3,\ i_{f_4}$), respectively.

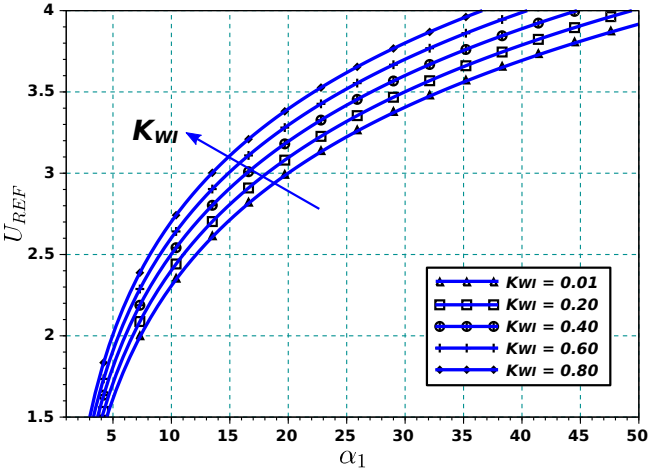


Figure 14: U_{REF} vs. α_1 for different values of K_{WI}.

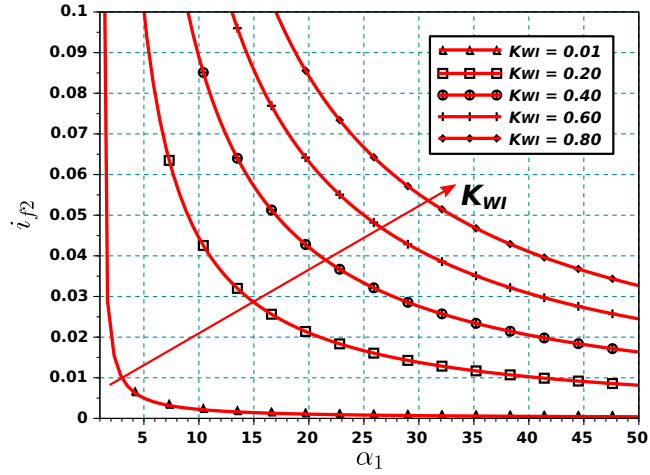


Figure 15: i_{f_2} vs. α_1 for different values of K_{WI}.

In Table 3, possible combinations of the specification to produce the K_{WI} values used in Fig. 14 and 15 are presented.

Table 3: ΔV_{REF} as function of $\Delta I_D/I_D$ and K_{WI}.

$\Delta I_D/I_D$ \ K_{WI}	**0.01**	**0.20**	**0.40**	**0.60**	**0.80**
4 %	5.18 μV	0.1 mV	0.21 mV	0.31 mV	0.41 mV
8 %	10.4 μV	0.21 mV	0.41 mV	0.62 mV	0.83 mV
12 %	15.5 μV	0.31 mV	0.62 mV	0.93 mV	1.24 mV
16 %	20.7 μV	0.41 mV	0.83 mV	1.24 mV	1.66 mV
20 %	25.9 μV	0.52 mV	1.04 mV	1.55 mV	2.07 mV

The design methodology of the self-biased current source can be represented by the simplified flowchart shown in Fig 16. The reference voltage V_{REF} is initially selected to maintain M_1 and M_3 in the linear region (less than $4\phi_t$). By establishing the acceptable error ΔV_{REF}, with the aid of (2.33),the coefficient K_{WI} is calculated, using the specification of the current mirror mismatch (ΔI_D). The value of α_3 is selected as high as possible to bias SCM deep in weak inversion ($i_{f_2} << 1$). If i_{f_2} is not lower enough, another acceptable error must be considered and α_1 and i_{f_2} recalculated.

The same value of V_{REF} is used to determine the inversion level i_{f_4}. By establishing the acceptable error Δi_{f_4}, with the aid of (2.20), the coefficient K_{MI} is calculated, using the specification of the input offset voltage of the operational amplifier (V_{OS}). In this case, α_1 is selected between the range of 1 and α_3. With this value, and depending on K_{MI}, the inversion level i_{f_4} is obtained. If these values are not appropriate, another acceptable error must be considered and α_3 and i_{f_4} recalculated.

With all the inversion levels and geometric ratios selected, the dimensions of all the SCM transistors can be calculated, depending of the desired output current (I_D), which depends of the specific application of the circuit. It is important to notice that in the design methodology, the parameters α_1 and α_3 are selected as integer numbers.

2.3.2 Stability Analysis

The proposed current source contains two feedback loops that can be easily identified in Fig. 9. The stability of the circuit is established if

the negative feedback network gain is higher than the positive feedback network gain. Looking at (2.30), if M_2 operates deep in weak inversion, (i.e. if i_{f_2} tends to zero) then the reference voltage is insensitive to current variations, resulting in $\Delta V_{REF} = 0$. For this reason, the SCM that operates with less inversion level must close the positive loop of the circuit and the intermediate node of the SCM that operates in moderate inversion must be connected to the non-inverting input of the operational amplifier, as shown in Fig. 17.

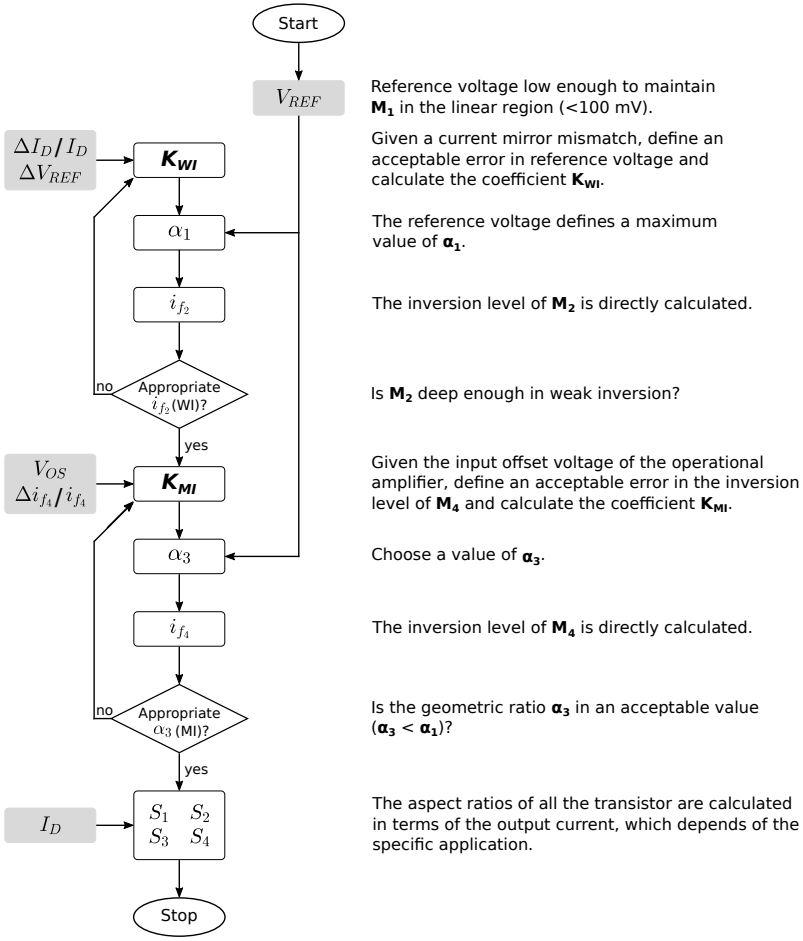


Figure 16: Flowchart used to design the self-biased current source.

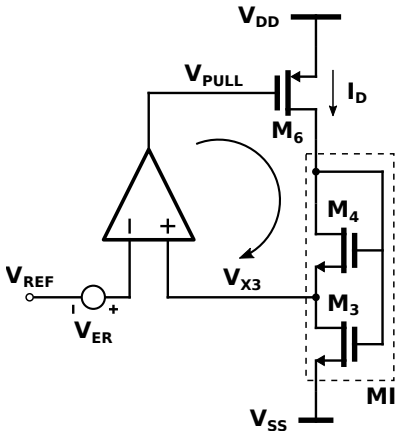


Figure 17: Negative feedback loop of the circuit.

2.3.3 Area Optimization

The proposed current source can be designed targeting a minimum area, considering that an area estimation can be obtained from the aspect ratios and the inversion levels of the SCMs transistors. From 2.1, the aspect ratio of the transistors in the linear region is:

$$S_{1,3} = \frac{I_D}{I_{SQ}\left(i_{f_{1,3}} - i_{r_{1,3}}\right)}, \tag{2.35}$$

and the aspect ratio of the saturated transistors is

$$S_{2,4} = \frac{I_D}{I_{SQ}\left(i_{f_{2,4}}\right)}. \tag{2.36}$$

The area of a single transistor can be expressed as

$$A = WL = SL^2. \tag{2.37}$$

If M_2 operates deep in weak inversion (i.e. $i_{f_2} << 1$), the aspect ratios are greater than 1, thus the SCM area formed by M_1 and M_2 is proportional to the sum of the aspect ratios of M_1 and M_2

$$A_{1,2} \propto S_1 + S_2 = \frac{S_2}{\alpha_1 - 1} + S_2 = S_2\left(\frac{\alpha_1}{\alpha_1 - 1}\right). \tag{2.38}$$

Using (2.33) and assuming $V_{REF} = \phi_t \ln(\alpha_1)$ results in

$$A_{1,2} \propto S_1 + S_2 = \frac{I_D}{I_{SQ}} \frac{1}{2K_{WI}} e^{\frac{V_{REF}}{\phi_t}}. \tag{2.39}$$

On the other hand, if M_4 operates in moderate inversion (i.e. $i_{f_4} \geq 1$), the aspect ratio are less than or equal than 1, thus the SCM area formed by M_3 and M_4 is proportional to the sum of the inverse of the aspect ratios of M_3 and M_4

$$A_{3,4} \propto \frac{1}{S_3} + \frac{1}{S_4} = \frac{\alpha_3 - 1}{S_4} + \frac{1}{S_4} = \frac{\alpha_3}{S_4}. \tag{2.40}$$

Replacing (2.25) produces

$$A_{3,4} \propto \frac{1}{S_3} + \frac{1}{S_4} = \frac{I_{SQ}}{I_D} i_{f_4} \alpha_3 = \frac{I_{SQ}}{I_D} i_{f_3}. \tag{2.41}$$

Finally, replacing (2.22) yields

$$A_{3,4} \propto \frac{1}{S_3} + \frac{1}{S_4} = \frac{I_{SQ}}{I_D} \left\{ \left[1 + K_{MI} \frac{e^{U_{REF} - K_{MI}}}{(e^{U_{REF} - K_{MI}}) - 1} \right]^2 - 1 \right\}. \tag{2.42}$$

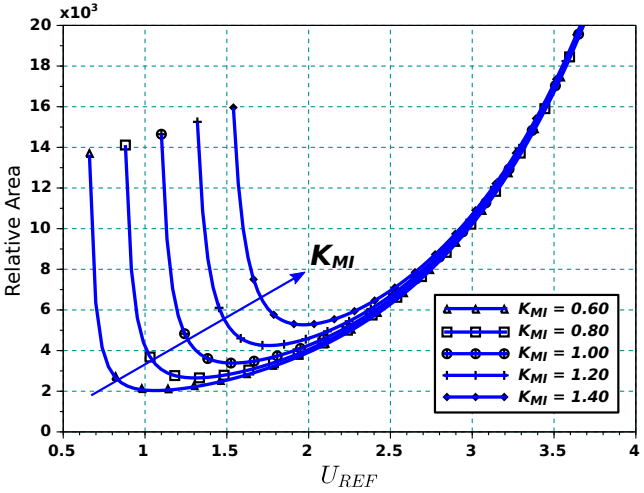


Figure 18: Relative area of the SCM for different values of K_{MI}.

It is clear that the total area of both SCMs depends strongly on the reference voltage. As it is clear from (2.39), the area of the SCM in weak inversion increases exponentially with V_{REF}. On the other hand, the area of the SCM in moderate inversion decreases with V_{REF}. Thus, there is an optimum value for V_{REF} which minimizes the total area of the circuit. For a particular design, the possible values of relative area in terms of the coefficient K_{MI} are presented in Fig. 18, where the arrow indicates the effect of increasing the value of K_{MI}.

2.4 CHAPTER SUMMARY

A design methodology of a modular CMOS ultra-low-power self-biased current source was developed based on the the ACM model in terms of the specifications of the sub-blocks of the circuit. The design space of the current source was described in terms of the input offset voltage of the operational amplifier and the current mismatch of the current mirror. With the obtained curves, a set of 8 current sources will be designed in the next chapter, using different combinations of values of α_1 and α_3.

3 CURRENT SOURCE SUB-BLOCKS DESIGN

Nano-ampere current reference circuits are commonly used in ultra-low-power circuits [6] [8] [23–25], some of them used in specific applications [26, 27]. In this chapter, the design of each sub-block of the current source is presented. According with (2.1), the aspect ratio of the SCM transistors, depends strongly on the desired output current. For a particular case, a 1 nA current source will be designed in this dissertation. The design of the SCMs is based on the methodology described in the previous chapter, assuming the admissible variations of the circuit are determined by the operational amplifier and the current mirror errors.

3.1 SELF-CASCODE MOSFETS

Each one of the SCMs are formed by the series and parallel association of unity transistors as shown in Fig. 19, increasing the matching between both structures and reducing the threshold voltage variations caused by imperfections in the fabrication process, including ion implantation, oxidation and etching [28]. As commented previously, one important feature of the SCMs is the choice of the geometrical parameters α_1 and α_3 as integer numbers in order to facilitate the placement in the layout.

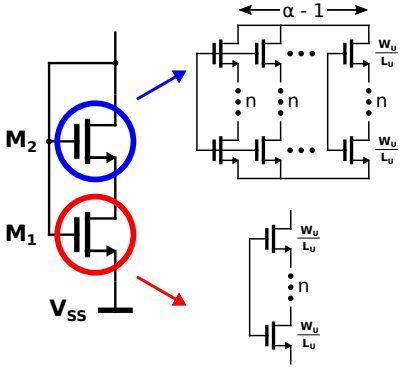


Figure 19: Series and parallel association in a SCM.

In the design of the SCM that operates in weak inversion, one design restriction was found. If $i_{f_2} << 1$, then the drain voltage of M_2 can be deduced from (2.7), using the first-order approximation (2.14):

$$V_{D2} = V_{G2} = V_{T0} + n\left\{V_{REF} + \phi_t\left[\frac{i_{f_2}}{2} - 1 + \ln\left(\frac{i_{f_2}}{2}\right)\right]\right\}. \quad (3.1)$$

With the extracted parameters presented in Appendix C, the calculated drain voltages for the SCM implemented with regular V_{T0} (thin oxide) and medium V_{T0} (thick oxide) NMOS transistors are those presented in Table 4, for two reference voltages $V_{REF} = 2\phi_t$ and $V_{REF} = 3\phi_t$.

Table 4: Drain voltages of SCM with regular and medium V_{T0} NMOS operating at different weak inversion levels.

		Regular V_{T0}	Medium V_{T0}
V_{REF}	i_{f_2}	V_{D2}	V_{D2}
$2\phi_t$	0.1	172 mV	396 mV
	0.01	110 mV	310 mV
	0.001	48 mV	225 mV
$3\phi_t$	0.1	199 mV	434 mV
	0.01	136 mV	348 mV
	0.001	74 mV	262 mV

If $i_{f_2} << 1$ the drain voltages of the regular V_{T0} transistor are not enough to maintain M_2 in saturation. Even in the most favorable case (i.e. $i_{f_2} = 0.1$), the drain voltage has a Complementary-to-Absolute Temperature (CTAT) behavior due to the strong dependence on V_{T0} [29], as shown in (3.1), and for high temperatures the transistor could not be in saturation anymore. Due to this issue, the best option to adequately explore the design space of the current source is using medium V_{T0} transistors to implement both SCMs.

Both reference voltages presented in Table 4 were selected to design a set of self-biased current sources. The maximum practical values of α_1 are 7 in the first case and 20 in the second case. The possible combinations of α_1 and α_3 were selected from the procedure presented in Chapter 2 and their values are presented in Table 5.

Table 5: Aspect ratio and inversion levels of the SCMs selected for 8 different current sources.

	Weak Inversion			Moderate Inversion		
V_{REF}	α_1	i_{f1}	i_{f2}	α_3	i_{f3}	i_{f4}
$2\phi_t$	7	0.261	0.0373	5	2.5	0.499
	7	0.261	0.0373	3	10.1	3.35
	6	1.14	0.19	3	10.1	3.35
	6	1.14	0.19	4	4.86	1.21
$3\phi_t$	19	0.242	0.0127	13	2.33	0.179
	19	0.242	0.0127	15	1.45	0.0965
	17	0.773	0.0455	11	3.52	0.32
	15	1.45	0.0965	11	3.52	0.32

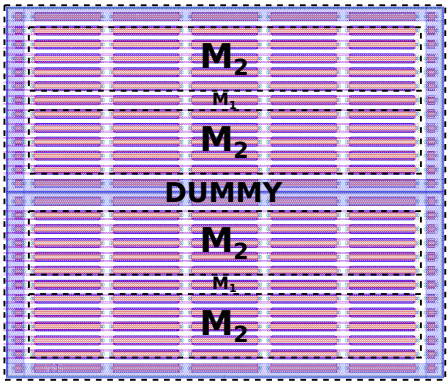
A typical layout of a SCM designed for one of the implemented current source is shown in Fig. 20. Unity transistors with multiple fingers arrangement and interdigitation were selected for these structures. In all of these transistors, the current is flowing in the same direction. Dummy transistors were used around the structure to resolve the edge effect problem and to improve the matching of the devices [28]. A guard-ring was connected around the structure to guarantee the adequate substrate polarization to avoid latch-up effects.

Despite using medium V_{T0} transistors in all of the SCM, the designed current sources were able to operate at supply voltages below 1 V as will be presented in Chapter 4.

3.2 OPERATIONAL AMPLIFIER

The operational amplifier used in the modular current source is a well-known PMOS input symmetrical Operational Transconductance Amplifier (OTA) [30] presented in Fig. 21. Due to the ultra-low-power requirement of the circuit, the OTA must be designed carefully, with transistors operating in weak and moderate inversion.

Instead of using series-parallel association [31], all of transistors of the current mirrors of the OTA are of the trapezoidal type [32], in



	W	L
M_1	400 nm	10x10 μm
M_2	10x400 nm	10x10 μm

Figure 20: Layout and dimensions of a typical SCM.

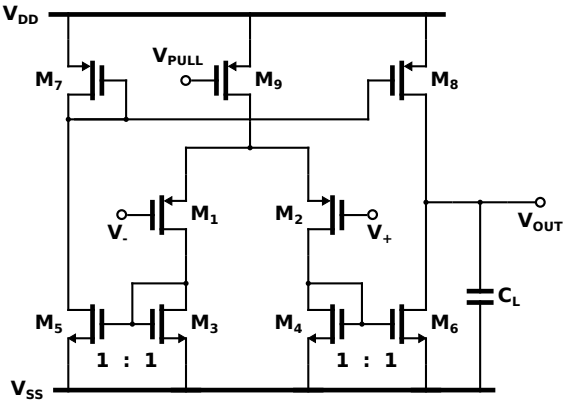


Figure 21: PMOS input symmetrical OTA.

order to obtain a high DC gain without the drawback of degradation of the frequency response which would result if the equivalent long-channel transistor were used. The trapezoidal transistor is an association of unity transistors connected as shown in Fig. 22. The equivalent dimensions are

$$W_{EQ} = mW_U \qquad L_{EQ} = (m+1)\,L_U, \tag{3.2}$$

where W_U and L_U are the width and length of the unity transistors.

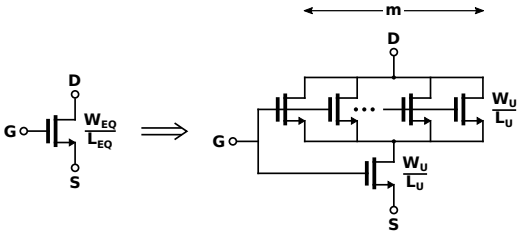


Figure 22: NMOS trapezoidal association.

The unity-gain frequency of the OTA in Fig. 21 is [16]

$$f_u = \frac{g_{m_{1,2}}}{2\pi C_L}. \tag{3.3}$$

Fig. 9 shows that the output of the OTA is loaded with the gates of the PMOS current mirror. Considering that the gate capacitance of these transistors cannot exceed 2 pF, and if the OTA is biased by the same nano-ampere output current, the unity-gain frequency of the OTA (f_u) could be limited in the range of kHz. In the situation where $f_u = 1$kHz, the resulting transconductance of the differential pair is

$$g_{m_{1,2}} = 2\pi f_u C_L = 12.56\ \frac{nA}{V}. \tag{3.4}$$

In the ACM model, the gate transconductance for a saturated transistor is expressed as [16]

$$g_m = \frac{2\ I_D}{n\phi_t} \frac{1}{\sqrt{1+i_f}+1}. \tag{3.5}$$

In order to increase the transconductance-to-current ratio, the differential pair operates in weak inversion. In the case of $i_{f_{1,2}} = 0.01$, the tail current of the OTA can be calculated using (3.5) as

$$I_{BIAS} = 2\ I_D = g_{m_{1,2}} n\phi_t \left(\sqrt{1+i_{f_{1,2}}}+1\right) = 0.929\ nA. \tag{3.6}$$

For the same reasons mentioned in Section 3.1, medium V_{T0} transistors were selected to design the OTA. An inconvenient of this amplifier is that both input voltages are near to ground potential ($2\phi_t$ and $3\phi_t$). Thus, source follower level shifters [33] were used on the input of the differential amplifier to increase the input voltages. This solution is shown in Fig. 23, where the source follower transistors (M_{L1} and

M_{L2}) are biased with two additional branches of the current source.

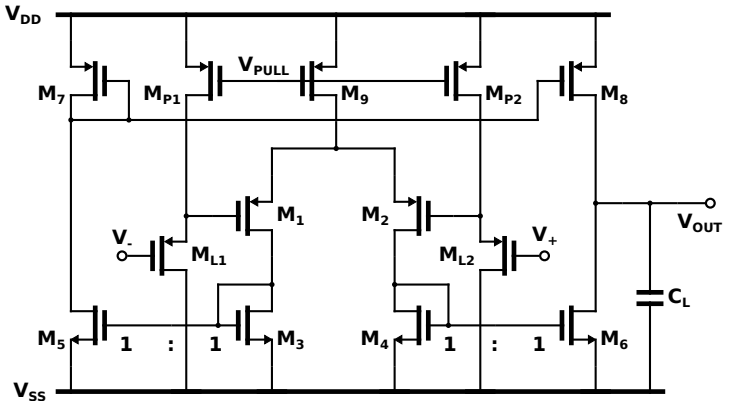


Figure 23: Symmetrical OTA with source follower level shifters.

In Table 6 the aspect ratios and the inversion levels of the transistors used in the OTA are summarized.

Table 6: Dimensions of the OTA transistors.

Transistor	i_f	W	L
$M_{1,2}$	0.01	4.8 μm	2 μm
$M_{L1,2}$	0.01	4.8 μm	2 μm
$M_{3,4,5,6}$	0.1	2.5 μm	20 μm
$M_{7,8,9}$	2	1 μm	20 μm
$M_{P1,2}$	2	1 μm	20 μm

The layout of the symmetrical OTA with source follower level shifters is presented in Fig. 24. All of the NMOS and PMOS current mirror transistors are distributed in interdigitated structures. The use of level shifters at the input of the OTA contributes to increase the input offset voltage. To alleviate this drawback, the source follower transistors have the same dimensions of the differential pair and they were placed in the same common centroid structure to increase the matching between them [28]. The details of the layout of the differential pair are presented in Fig 25.

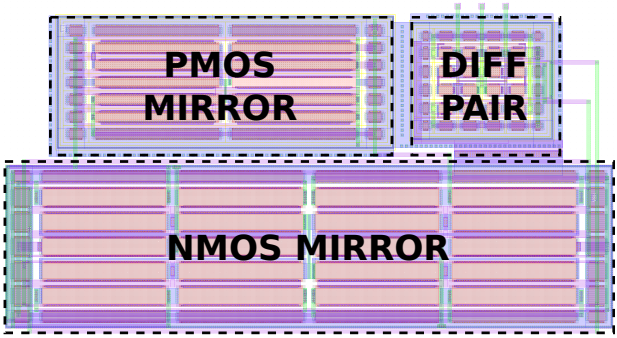


Figure 24: Layout of the symmetrical OTA.

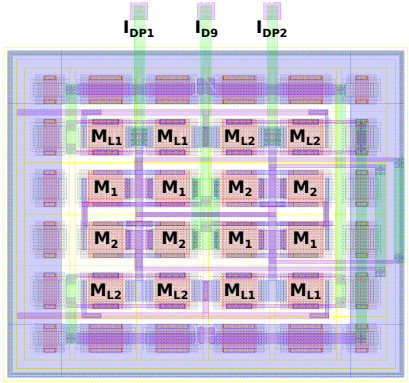


Figure 25: Layout of the input differential pair and source follower transistors.

3.2.1 Input Offset Voltage

The input offset voltage (V_{OS}) of the OTA represents the transistor mismatches and corresponds to the differential input voltage required for the output current to be equal to zero [16]. The standard deviation of the offset voltage of a differential pair can be calculated using the Pelgrom's model of mismatch [16] [34] as

$$\sigma^2\left(V_{OS}\right) = \frac{A_{VT}^2}{WL} + \left(\frac{I_D}{g_m}\right)^2 \frac{A_\beta^2}{WL}, \tag{3.7}$$

where A_{VT}^2 is the threshold mismatching coefficient and A_β^2 is the specific current mismatching coefficient, both depending on technological parameters. Replacing (3.5) in (3.7) yields

$$\sigma^2\left(V_{OS}\right) = \frac{A_{VT}^2}{WL} + \left(n\phi_t \frac{\sqrt{1+i_{f_{1,2}}}+1}{2}\right)^2 \frac{A_\beta^2}{WL}. \tag{3.8}$$

The input offset voltage is proportional to the inverse square root of the transistor area. If the differential pair transistors operate in the weak inversion, the specific current mismatch is minimized.

The input offset voltage of the circuit presented in Fig. 21 corresponds to the threshold voltage mismatch of the differential pair in addition of the mismatches of the pairs $M_3 - M_4$, $M_5 - M_6$ and $M_7 - M_8$. Assuming that the specific current mismatch does not play an important role, V_{OS} is mostly affected by the threshold voltage mismatches [16], yields

$$\sigma^2\left(V_{OS}\right) \approx \frac{A_{VT_P}^2}{WL_{1,2}} + \left(\frac{g_{m_{3,4}}}{g_{m_{1,2}}}\right)^2 \frac{A_{VT_N}^2}{WL_{3,4}} + \left(\frac{g_{m_{5,6}}}{g_{m_{1,2}}}\right)^2 \frac{A_{VT_N}^2}{WL_{5,6}} + \left(\frac{g_{m_{7,8}}}{Bg_{m_{1,2}}}\right)^2 \frac{A_{VT_P}^2}{WL_{7,8}}. \tag{3.9}$$

3.3 CURRENT MIRROR

The simple PMOS current mirror presented in Fig. 26 is used in the current source to copy the current from a branch to another. For simplicity, a unity-gain current mirror was used, but the design can be extended to different current proportionality factors.

Although the current mirror is formed by identical transistors, inaccuracies in current mirroring are mainly caused by mismatch in their threshold voltages caused by process variations, and differences between their drain voltages produced by the channel modulation effect [22].

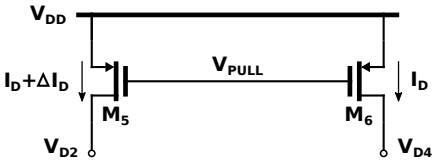


Figure 26: PMOS current mirror.

The layout of the current mirror is presented in Fig. 27. Additional branches used to bias the OTA and the level shifters are included in the structure, where all the transistors were placed in interdigitated distribution with identical separations between them to mitigate the mismatch and process variation effects. PMOS unity transistors of 1 μm/40 μm were used to design the current mirrror. M_{P1} and M_{P2} transistors correspond to the series association of two unity transistors to decrease in half the reference current to bias the level shifters.

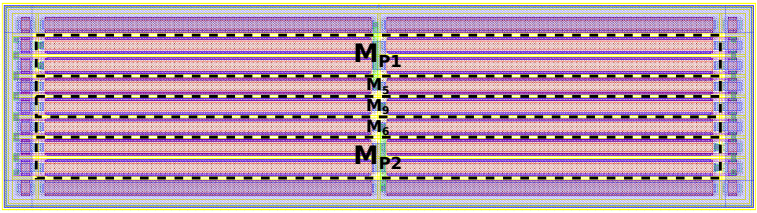


Figure 27: Layout of the PMOS current mirror.

3.4 START-UP

Due to the metastable nature of the self-biased current source, two possible stable states exist [22]: one corresponds to the quasi-equilibrium or zero-bias state, and the other corresponds to the desirable equilibrium state. To ensure that the current source is biased in the stable equilibrium state, the negative feedback gain of the current source must be dominant over the positive feedback gain. The common mechanism to guarantee this condition is using a start-up sub-block [35].

For the designed current source, the start-up proposed is presented in Fig. 28. The capacitor C_{ST} is slowly charged through P_1 whereas the V_{PULL} node is pulled to ground, forcing the current mirror to drive current in both SCMs until the inverter formed by N_1 and P_3 changes its output state. At this point, the node V_{PULL} is released, and C_{ST}

rapidly reaches V_{DD} due to the action of P_2. In this way the start-up stops driving current and the OTA correctly closes the loop reducing the positive feedback gain, bringing the circuit to the desired equilibrium state where the start-up has no effect anymore. Despite this circuit is operating in open loop configuration (no one internal voltage node of the current source is being tracked), the current source reaches the stable state in a relative short period.

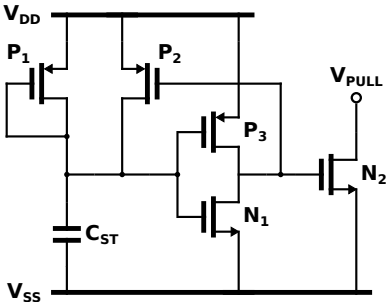


Figure 28: Start-up circuit.

The layout of the start-up is presented in Fig. 29. The capacitor C_{ST} was implemented with 9 NMOS transistors connected in parallel. The start-up structure is not very susceptible to mismatch, however the routing and placement of the components were carefully chosen.

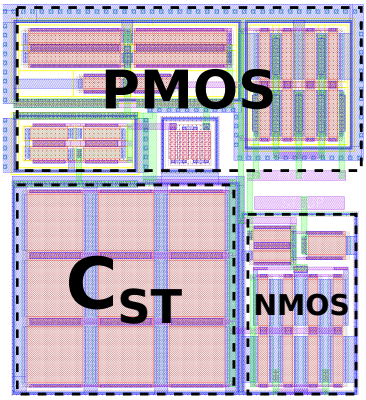


Figure 29: Layout of the start-up.

3.5 CHAPTER SUMMARY

All the sub-blocks of the CMOS ultra-low-power self-biased current source were designed, using the input specifications and defining some restrictions, in the particular case of the unity-gain frequency of the OTA. The schematic and layout of these sub-blocks were carefully designed to minimize the mismatch variations. To evaluate the performance of these sub-blocks and the complete current source, various simulations were performed. Simulation results will be presented in the next chapter.

4 SIMULATION RESULTS

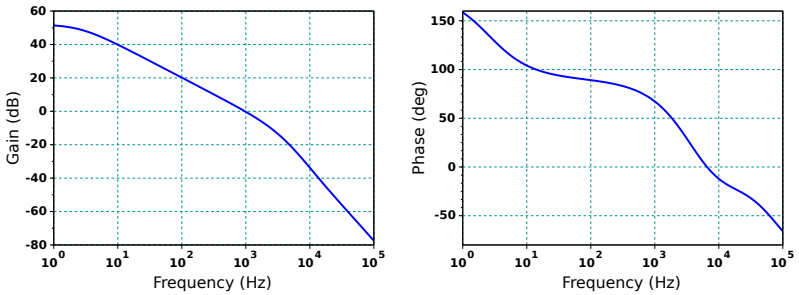
In this chapter, the schematic and post-layout simulation results of the current source are presented to validate the design methodology described in Chapter 2. Different simulations were performed to measure the main parameters of the sub-blocks and the complete circuit. The obtained results will later serve to determine the performance of the circuit.

4.1 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Basic simulations to measure the main parameters of the OTA were performed. Despite the input offset voltage is the higher source of errors in the current source and the OTA is going to be used in DC condition, these main parameters were obtained using AC simulation.

4.1.1 AC Simulation Results

An AC simulation was used to verify the main features of the OTA in the frequency domain. In this simulation, the DC gain, the phase margin and the unity-gain frequency were measured. The results of the post-layout simulation are presented in Fig. 30.



(a) (b)

Figure 30: AC simulation results of the OTA: (a) gain, and (b) phase.

A relative high gain OTA is desirable to equalize the intermediate voltages of both SCMs and remain the closed loop in the stable state.

Typical simulations showed that the amplifier has a DC gain of 51.39 dB, a phase margin of 67.97°, a unity-gain frequency of approximately 1 kHz, consuming only 3 nA.

4.1.2 Statistical Simulation Results

A Monte Carlo sampling simulation was performed to measure the input offset voltage of the OTA caused by both random errors and systematic errors, the latter caused by the amplifier asymmetry. One thousand simulations were run to obtain the statistical results. In Fig. 31 the histogram of the obtained variations of the input offset voltage of the OTA is presented. The obtained input offset voltage for 3σ variation is near 5 mV. This is a good value, because it was shown in the design methodology presented in Chapter 2 that such results are coherent with the specifications selected.

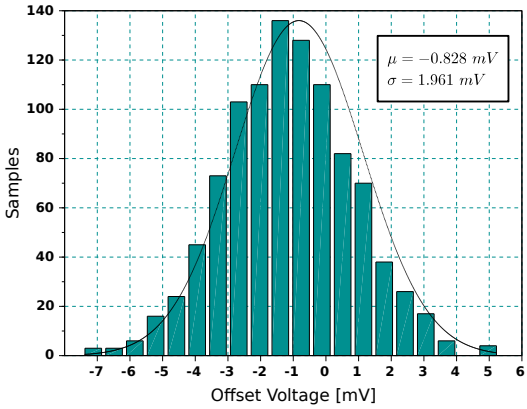


Figure 31: Monte Carlos simulation results for the OTA input offset voltage.

4.2 CURRENT SOURCE

According to the design methodology, a set of 8 current sources were designed with geometric ratios, inversion levels, and reference voltages as summarized in Table 5. The circuits were designed to

generate a 1 nA output current, having a quiescent current of 5 nA.

4.2.1 DC Simulation Results

To measure the supply voltage dependence of the current source, a DC simulation was performed by sweeping the value of the V_{DD} from 0 to 2 V. In Fig. 32 and Fig. 33, the DC simulation results for the 4 current sources designed with $V_{REF} = 2\phi_t$ are presented. In Table 7 these results are summarized.

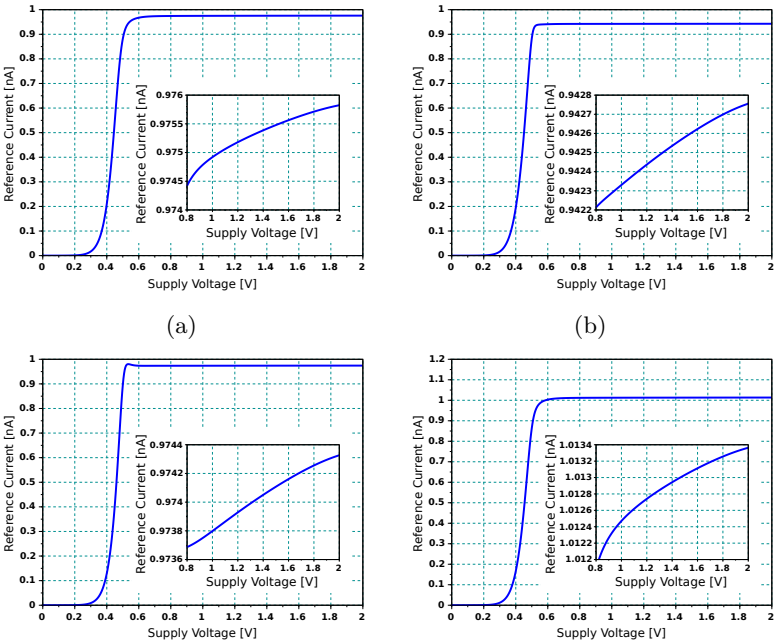


Figure 32: Reference current of the 4 current sources with $V_{REF} = 2\phi_t$.

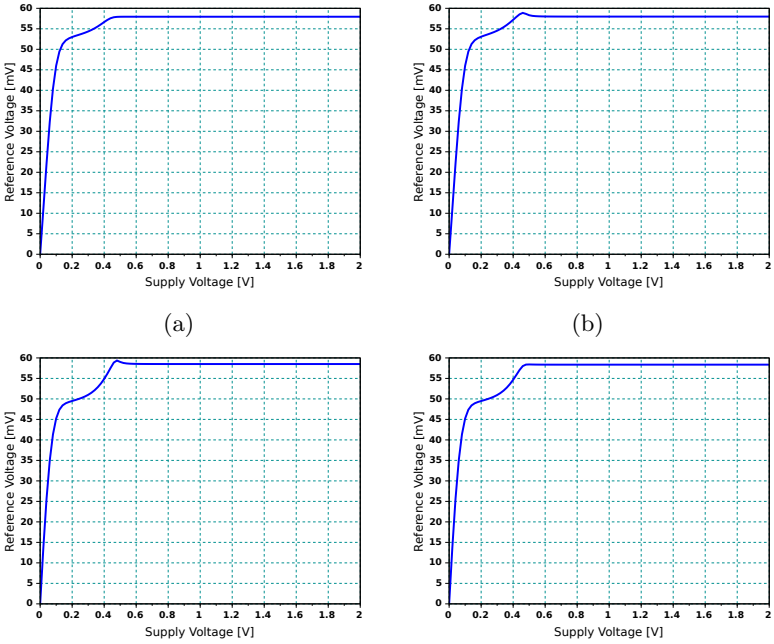


Figure 33: Reference voltage of the 4 current sources with $V_{REF} = 2\phi_t$.

Table 7: DC simulation results for the current sources with $V_{REF} = 2\phi_t$.

α_1	α_3	I_D	V_{REF}	Line Regulation
7	5	0.975 nA	57.95 mV	0.11 %/V
7	3	0.942 nA	57.98 mV	0.05 %/V
6	3	0.974 nA	58.51 mV	0.06 %/V
6	4	1.013 nA	58.36 mV	0.11 %/V

In Fig. 34 and Fig. 35, the DC simulation results for the 4 current sources designed with $V_{REF} = 3\phi_t$ are presented. In Table 8 these results are summarized.

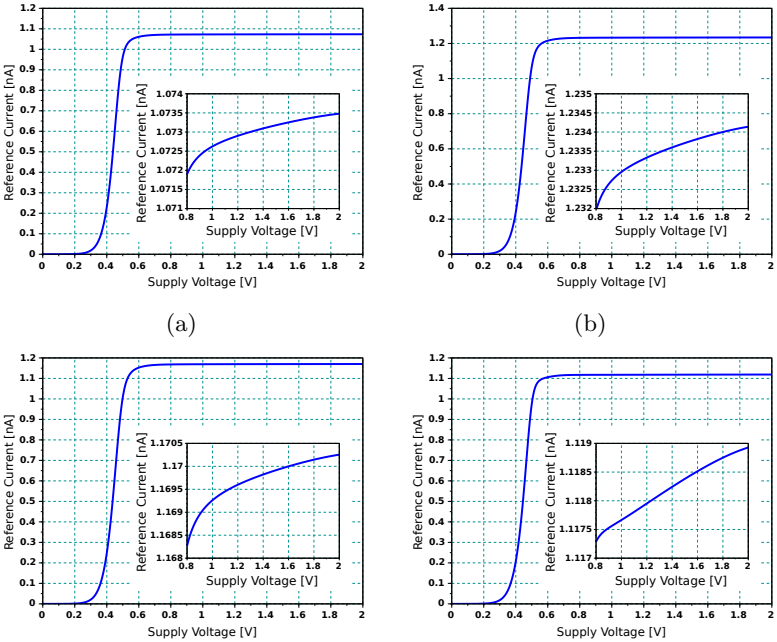


Figure 34: Reference current of the 4 current sources with $V_{REF} = 3\phi_t$.

Table 8: DC simulation results for the current sources with $V_{REF} = 3\phi_t$.

α_1	α_3	I_D	V_{REF}	Line Regulation
19	13	1.073 nA	88.91 mV	0.12 %/V
19	15	1.233 nA	89.22 mV	0.1 %/V
17	11	1.169 nA	89.13 mV	0.09 %/V
15	11	1.118 nA	88.82 mV	0.13 %/V

In most of designed current sources, a fine tune in the width of the SCM transistors was performed to adjust the value of the reference current near to 1 nA. However, none of the designed current sources produced the selected reference voltage. One possible cause is the inaccuracy of the transistor model used by the simulator.

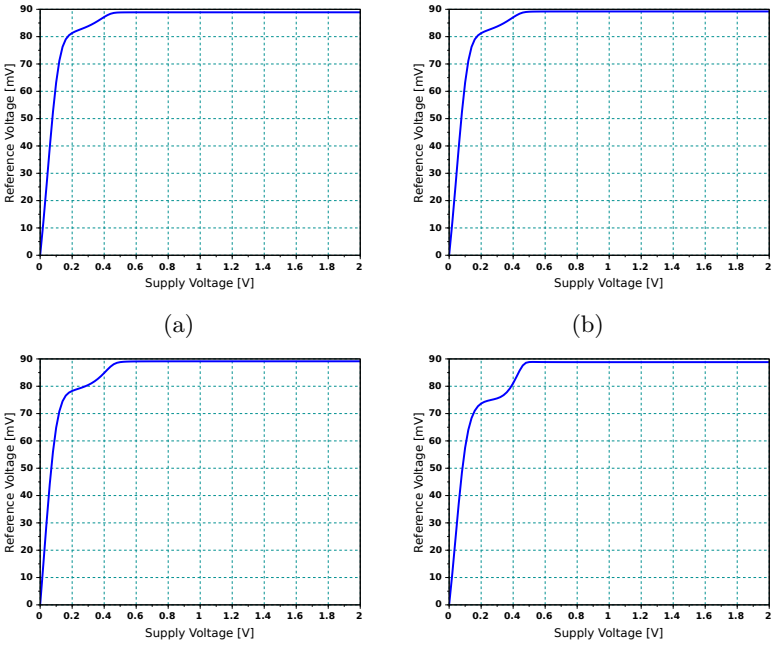


Figure 35: Reference voltage of the 4 current sources with $V_{REF} = 3\phi_t$.

Fig. 36 shows the dependence of the reference current on both temperature and process spreading. As it was previously mentioned, the output current is proportional to the specific current of M_4. According to (2.2), and from the parameter extraction presented in Appendix C, this current approximates a PTAT behavior, showing that the mobility has an approximate negative linear dependence with the temperature.

4.2.2 Statistical Simulation Results

To validate the design methodology, two current sources with the same reference voltage and different geometric ratios were selected to compare their performance and determine the influence of different values of α_3. The two selected current sources have the following geometric ratios: i) $\alpha_1 = 7$ and $\alpha_3 = 5$, and ii) $\alpha_1 = 7$ and $\alpha_3 = 3$.

Fig. 37 shows the Monte Carlo simulation results for the reference

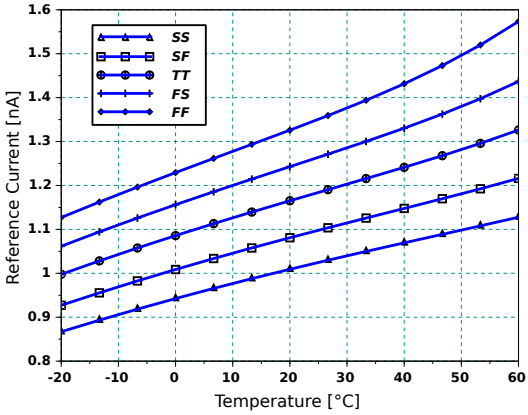
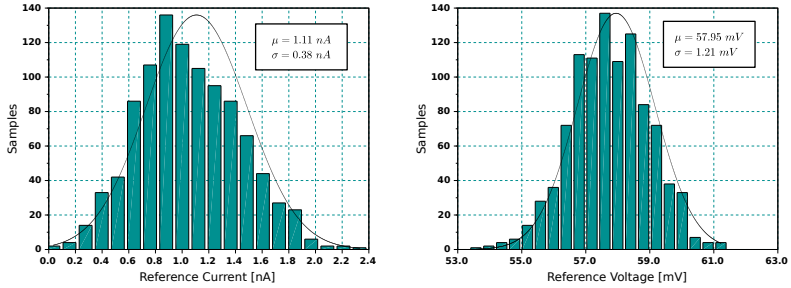


Figure 36: Temperature dependence of I_D with $V_{REF} = 2\phi_t$.

current (I_D) and the reference voltage (V_{REF}) for the current source with $V_{REF} = 2\phi_t$, $\alpha_1 = 7$ and $\alpha_3 = 5$. The circuit is very sensitive to variations in I_D caused by the voltage error V_{ER}. Unlike this, the reference voltage is less sensitive to mismatch and process variations (a standard variation of 1.21 mV only).

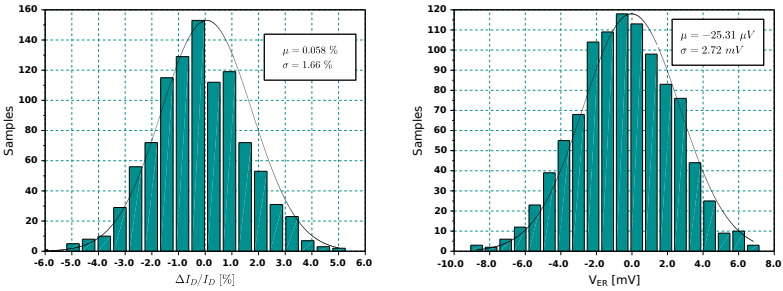


(a) (b)

Figure 37: Monte Carlo simulation results for: (a) I_D, and (b) V_{REF} with $\alpha_1 = 7$ and $\alpha_3 = 5$.

The Monte Carlo simulation results were also employed to validate the statistical results of the current source with the admissible errors used to describe the design space in Chapter 2. In Fig. 38, the statistical simulation results for $\Delta I_D/I_D$ and V_{ER} are presented. It is clear that

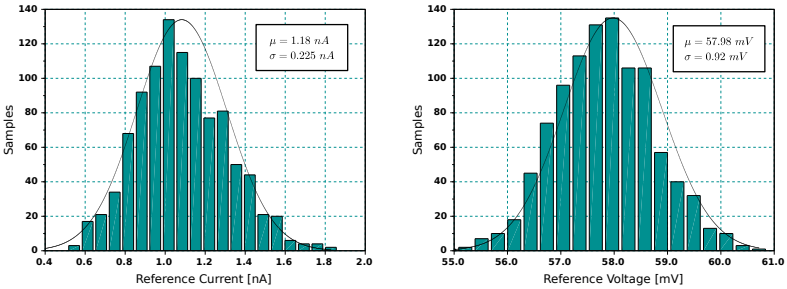
the values obtained for $\Delta I_D/I_D$ are less than those used to define the design space. Also, it is important to notice that V_{ER} includes the contribution of the input offset voltage of the OTA and the threshold voltage mismatch of the SCM transistors. The direct effect of V_{ER} is the variation in the reference current defined by M_4, because as was anticipated in Chapter 2, the maximum variations in the inversion level of M_4 can be as high as 50% for an input voltage of 5 mV.



(a) (b)

Figure 38: Monte Carlo simulation results for: (a) $\Delta I_D/I_D$ and (b) V_{ER} with $\alpha_1 = 7$ and $\alpha_3 = 5$.

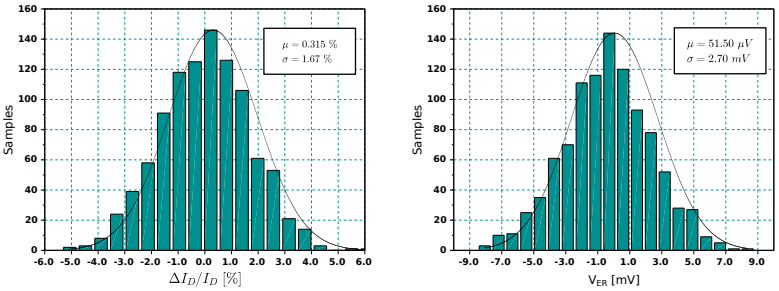
Fig. 39 shows the Monte Carlo simulation results for I_D and V_{REF} for the current source with $V_{REF} = 2\phi_t$, $\alpha_1 = 7$ and $\alpha_3 = 3$. The circuit is a little less sensitive to variations in I_D, with a reduction in the standard variation of the reference current of 0.38 nA to 0.225 nA.



(a) (b)

Figure 39: Monte Carlo simulation results for: (a) I_D, and (b) V_{REF} with $\alpha_1 = 7$ and $\alpha_3 = 3$.

In Fig. 40, the statistical simulation results for $\Delta I_D/I_D$ and V_{ER} are presented. The values obtained of $\Delta I_D/I_D$ and V_{ER} are very similar to those obtained in the previous case because the same SCM in weak inversion was used to generate V_{REF}.



(a) (b)

Figure 40: Monte Carlo simulation results for: (a) $\Delta I_D/I_D$ and (b) V_{ER} with $\alpha_1 = 7$ and $\alpha_3 = 3$.

4.3 START-UP

The start-up circuit, which provides a stimulus to bring the current source to the desired equilibrium state, was tested for both fast and slow variations of the supply voltage.

4.3.1 Transient Simulation Results

To test the start-up appropriately, transient simulations were run for V_{DD} increasing linearly from 0 to 2 V. Two cases were considered: i) the V_{DD} ramp rises quickly in an interval of 100 μs, and ii) the ramp rises slowly rising in an interval of 10 ms.

For the first case, shown in Fig. 41, it is observed that (in a short period time) the current mirror forces a high transient current to flow through the SCM branches, until a certain supply voltage value is reached. At this point, the current through N_2 tends to zero, the start-up stops consuming current, and the OTA closes the loop in the stable state, adjusting the output current in the designed value.

For the second case, shown in Fig. 42, it is observed that (also in

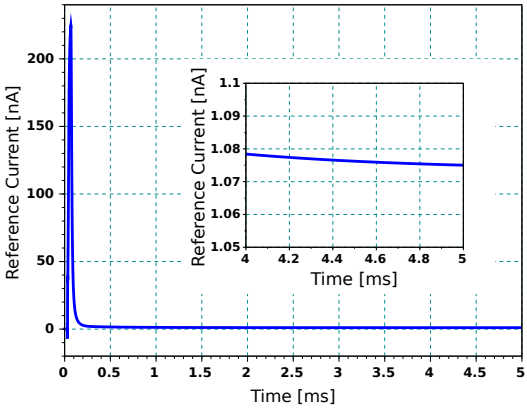


Figure 41: Output current with the influence of the start-up with a fast ramp in V_{DD} .

a relative short period time) the current mirror is forced to drive current through the SCMs. Due to the slow change in V_{DD}, the transient current is lower than in the first situation. Also in this case, meanwhile the supply voltage reaches the maximum value, the OTA closes the loop in the stable state; however, in this case, the settling time of the current source is higher.

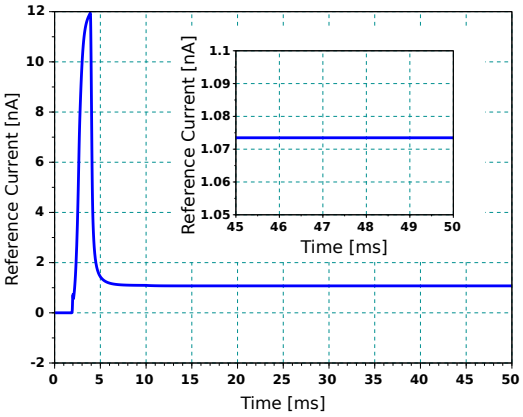


Figure 42: Output current with the influence of the start-up with a slow ramp in V_{DD}.

Despite the current source reaches the stable state by the effect of the start-up, the initial transient current goes to values higher than 200 nA when the supply voltage rises in a short interval of time. This effect can be removed designing a start-up with closed loop configuration to track some internal voltage nodes of the current source and reduce the transient current peak.

By removing the start-up of the current source, the difference of the circuit response becomes very slow. Fig. 43 shows that, if the start-up is not included, the settling time of the current source is much higher in comparison with the two latter situations, independently of the supply voltage ramp duration. The OTA slowly closes the loop in the stable state because the SCMs are charged with a small amount of current. Since the current source is employed to bias another circuits, a design requirement to improve its performance is to reduce the settling time.

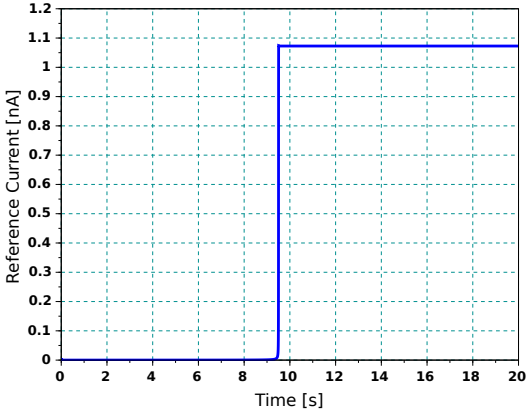


Figure 43: Output current without the influence of the start-up.

4.4 CHAPTER SUMMARY

A set of 8 self-biased current sources were simulate to validate the design methodology and the performance of the circuit. AC and Monte Carlo simulations were performed to evaluate the main features of the OTA. DC simulation results of the 8 designed current sources were presented, showing that the variation in the output current is strongly

dependent on the input offset voltage. However, the variation can be slightly reduced choosing an adequate value of α_3. Finally, transient simulation results demonstrate the importance of using a start-up in this circuit to avoid the operation of the current source in the zero-bias state.

5 CONCLUSIONS AND FUTURE WORKS

5.1 CONCLUSIONS

In this dissertation, a design methodology of an ultra-low-power self-biased current source using modular sub-blocks has been developed. The design procedure is based on the specifications of the sub-blocks and the admissible errors produced by the random variations of the matched transistors. A design space of the current source in terms of these errors was presented, where the dimensions and the inversion levels of all the SCM transistors were calculated using the equations of the ACM model, which describe all the operation regions of the transistor.

Different simulations were performed to validate the design methodology and the performance of the designed current sources. Monte Carlo analysis allowed to estimate the main design parameters, the input offset voltage of the OTA and the mismatch in the current mirror, generated by process variations. As expected, the deviations in the reference current were slightly reduced by increasing the inversion level of transistor M_4, and, as a consequence, reducing the geometric ratio α_3. In some cases this improvement is not feasible because it would be necessary to use too many transistors in series association, increasing the total area of the circuit.

AC and DC simulations were also performed to verify the performance of each one of the sub-blocks and the operation of the complete circuit Even though this circuit mostly operates in DC condition, the AC parameters will determine the stability of the circuit owing the current source contains two feedback loops. A relative high DC gain is desirable to obtain a more accurate response in the closed loop configuration, whereas an appropriate phase margin is needed to avoid oscillations. The symmetrical OTA designed in the dissertation allowed to satisfy these two conditions.

Temperature and supply voltage dependence of the current source were measured using DC simulations. In the first case, the output current has an approximate PTAT dependence, as described in Chapter4. On the other hand, using an OTA instead of a VFCM, the transfer of the intermediate voltage is more accurate and the line regulation can be improved.

In this type of circuits where a positive feedback loop is involved. the use of an additional sub-block to bring the circuit in the desirable equilibrium state is fundamental. Although the designed start-up pro-

duced the expected results, this circuit has some restrictions because it operates in a open loop configuration. To reduce the high transient current generated by the start-up, a closed loop configuration must be implemented.

A set of 8 current sources were designed to generate a 1 nA output current, with a quiescent current of 5 nA for each current source. Depending of the application, the output current is selected, and the dimensions of the SCM transistors will be calculated according to this value. In this particular situation, the designed output current will serve to bias some blocks used in ultra-low-power systems. Currently current source topology is being used in a project in progress developed by a master student of the Integrated Circuits Laboratory (LCI) in the Federal University of Santa Catarina (UFSC), consisting in a MOSFET-based radiation dosimeter.

5.2 FUTURE WORK

One of the limitations of the designed current source is the low value of the reference voltage, which increases the errors of the circuit. A way to reduce this error could be to increase this voltage by stacking a set of matched SCMs, as described in [15]. Using this technique, the source follower level shifters would not be necessary in the input of the OTA and the input offset voltage could be reduced. Other OTA topologies, additional improvements in the layout and offset cancellation techniques could be explored to reduce the input offset voltage.

To reduce the deviations in the current that flows across the two branches of the circuit, a cascode current mirror topology could be implemented, improving the PSRR of the circuit. The negative impact of this implementation is the increasing of the minimum supply voltage. Another aspects related to stability and noise of the current source are subject of future studies.

To improve the transient response of the current source and reduce the high current peak, a start-up block with closed-loop configuration must be explored, when some internal voltage node of the current source is tracked.

Finally, to fully validate the design methodology, a set of 8 current sources designed in GlobalFoundries CMOS 130 nm were submitted for fabrication through MOSIS Educational Program. Measurements will be performed in the laboratory to compare the experimental results with the post-layout simulation results.

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APPENDIX A – ERRORS IN THE CURRENT SOURCE

The operational amplifier and the SCMs introduce errors in the current source due to the input offset voltage and the threshold voltage mismatch, as a direct consequence of process imperfections and mismatch problems. In this appendix the effect of these variations in the inversion level of the saturated transistor M_4 is deduced.

A.1 ERRORS DUE TO THE INPUT OFFSET VOLTAGE OF THE OPERATIONAL AMPLIFIER AND THE THRESHOLD VOLTAGE MISMATCH OF THE SCM TRANSISTORS

The mismatch between M_3 and M_4 is represented by the difference between the threshold voltages as

$$\Delta V_{T0} = V_{T0_4} - V_{T0_3}. \tag{A.1}$$

From (2.7), the intermediate voltage V_{X3} in Fig. 9, including the threshold voltage mismatch, is

$$V_{X3} = \phi_t \left[F\left(\alpha_3\ i_{f_4}\right) - F\left(i_{f_4}\right)\right] + \frac{V_{T0_3} - V_{T0_4}}{n}. \tag{A.2}$$

Introducing the effect of the input offset voltage, the intermediate voltage becomes

$$V_{X3} + V_{OS} + \frac{\Delta V_{T0}}{n} = \phi_t \left\{F\left[\alpha_3 \left(i_{f_4} + \Delta i_{f_4}\right)\right] - F\left(i_{f_4} + \Delta i_{f_4}\right)\right\}. \tag{A.3}$$

The error voltage source V_{ER} connected to the inverting input of the operational amplifier corresponds to the contribution of the input offset voltage of the operational amplifier and the mismatch of the SCM transistors. By doing the linear interpolation around i_{f_4}, yields

$$V_{X3} + V_{ER} = \phi_t \left[F(\alpha_3\ i_{f_4}) + F'(\alpha_3\ i_{f_4})\left(\alpha_3\ \Delta i_{f4}\right)\right] - \phi_t \left[F(i_{f_4}) + F'(i_{f_4})\left(\Delta i_{f4}\right)\right]. \tag{A.4}$$

The variation caused by the offset voltage can be easily identified as

$$V_{ER} = \phi_t \left[F'(\alpha_3\ i_{f_4})\left(\alpha_3\ \Delta i_{f4}\right)\right] - \phi_t \left[F'(i_{f_4})\left(\Delta i_{f4}\right)\right]. \tag{A.5}$$

Replacing the derivatives of the function results in

$$V_{ER} = \frac{\phi_t}{2}\left\{\frac{\alpha_3\ \Delta i_{f_4}}{\sqrt{1+\alpha_3\ i_{f_4}}-1} - \frac{\Delta i_{f_4}}{\sqrt{1+i_{f_4}}-1}\right\}, \tag{A.6}$$

and simplifying (A.6) yields

$$V_{ER} = \frac{\phi_t}{2}\frac{\Delta i_{f_4}}{i_{f_4}}\left(\sqrt{1+\alpha_3\ i_{f_4}} - \sqrt{1+i_{f_4}}\right). \tag{A.7}$$

Since the input offset voltage is the dominant source error of the circuit, a valid approximation is $V_{ER} \approx V_{OS}$, given as result (2.17).

APPENDIX B – LAYOUT OF THE SUBMITTED INTEGRATED CIRCUITS

A set of 8 current sources were designed in GlobalFoundries CMOS 130 nm and submitted for fabrication hrough MOSIS Educational Program. In this appendix, the layout of two designed current sources are presented. The other current sources have similar dimensions, and the distribution of the sub-blocks is the same.

B.1 COMPLETE CURRENT SOURCE

In Fig. 44, the layout of a current source with $V_{REF} = 2\phi_t$, $\alpha_1 = 7$ and $\alpha_3 = 5$ is presented, with an occupied area of 0.0213 mm^2

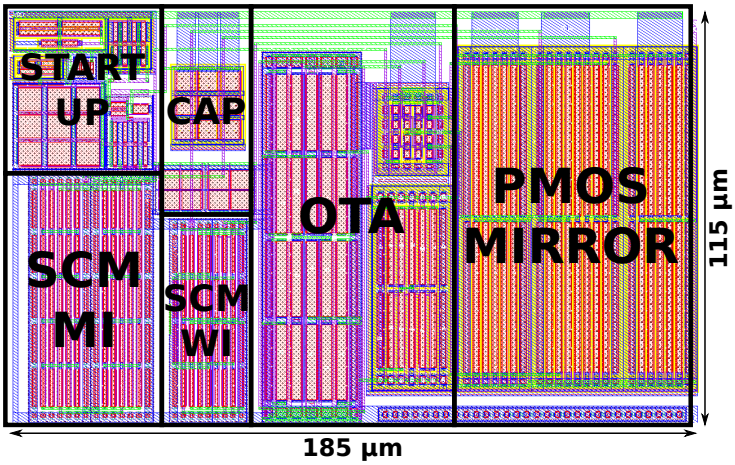

Figure 44: Layout of a current source with $V_{REF} = 2\phi_t$.

In Fig. 45, the layout of a current source with $V_{REF} = 3\phi_t$, $\alpha_1 = 15$ and $\alpha_3 = 11$ is presented, with an occupied area of 0.028mm^2.

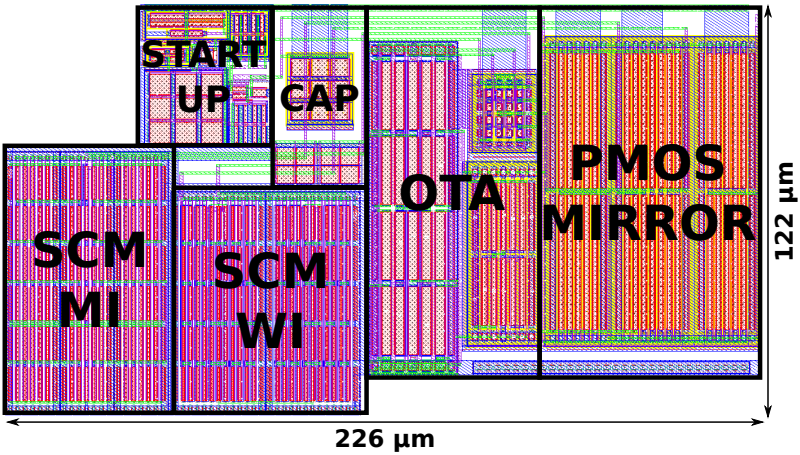

Figure 45: Layout of a current source with $V_{REF} = 3\phi_t$.

In Table 9, the area of each designed current source current is presented.

Table 9: Total Area of each one of the designed current sources.

V_{REF}	α_1	α_3	Width	Length	Area
$2\phi_t$	7	5	185 μm	115 μm	0.021 mm^2
	7	3	185 μm	115 μm	0.021 mm^2
	6	3	185 μm	115 μm	0.021 mm^2
	6	4	193 μm	115 μm	0.022 mm^2
$3\phi_t$	19	13	231 μm	115 μm	0.027 mm^2
	19	15	240 μm	115 μm	0.028 mm^2
	17	11	234 μm	115 μm	0.027 mm^2
	15	11	226 μm	122 μm	0.028 mm^2

APPENDIX C – PARAMETER EXTRACTION OF THE CMOS GLOBALFOUNDRIES 130 NM TRANSISTORS

In this appendix, the parameter extraction procedure of regular and medium V_{T0} transistors of the GlobalFoundries CMOS 130 nm technology (i.e. the one used in this master dissertation) is presented, according to the parameter extraction methodology described in [16] and [36]. The main parameters of the transistor (namely, V_{T0}, I_{SQ}, and n) were extracted from the g_m/I_D vs V_G characteristic curve of the circuit configuration presented in Fig. 46.

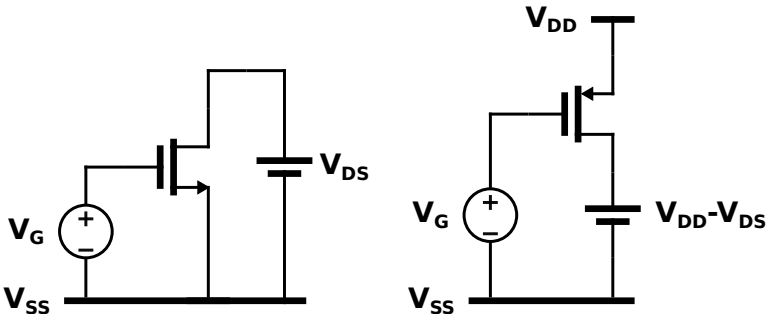

Figure 46: Circuit configuration for the parameter extraction.

In the g_m/I_D vs V_G curve, the point where g_m/I_D drops around half (53.1%) of its peak value is measured. The gate voltage obtained at this point is V_{T0} and the corresponding current is 0.88 I_{SQ} W/L. The same configuration was used for both type of transistors, with $V_{DS} = \phi_t/2$. For measuring the temperature dependence of the specific current of the transistors, a DC simulation with temperature sweeping was performed in the range between -20°C and 60°C, using a PTAT drain-to-source voltage source.

C.1 REGULAR V_{T0} (THIN OXIDE) TRANSISTOR

In Fig. 47 the characteristic g_m/I_D vs V_G curve of a 1 μm/1 μm regular V_{T0} NMOS transistor is presented. The circle corresponds to the point which $g_m/I_D = 0.531\,(g_m/I_D)_{max}$.

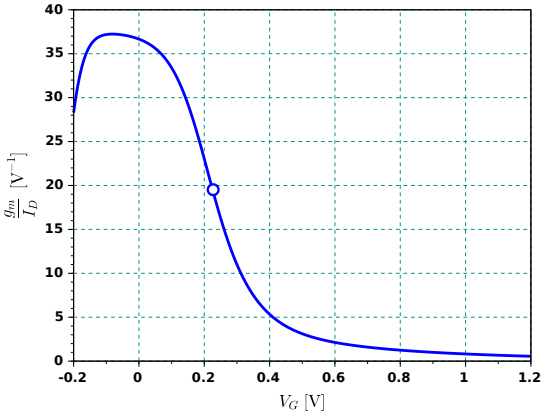

Figure 47: Transconductance-to-current of a regular V_{T0} NMOS vs. gate voltage for $V_{DS} = \phi_t/2$.

Table 10: Simulated parameters of regular V_{T0} NMOS transistor for different aspect ratios.

Parameter	1μm/1μm	1μm/2μm	1μm/5μm	1μm/10μm
V_{T0}	223.8 mV	205.2 mV	193.5 mV	189.8 mV
I_{SQ}	191.8 nA	196.6 nA	201.8 nA	205 nA
n	1.038	1.039	1.041	1.045

Table 11: Simulated parameters of regular V_{T0} PMOS transistor for different aspect ratios.

Parameter	1μm/1μm	1μm/2μm	1μm/5μm	1μm/10μm
V_{T0}	258.5 mV	248.4 mV	243 mV	241.9 mV
I_{SQ}	37.11 nA	36.72 nA	36.72 nA	37.13 nA
n	1.207	1.199	1.199	1.203

C.2 MEDIUM V_{T0} (THICK OXIDE) TRANSISTOR

In Fig. 48 the characteristic g_m/I_D vs V_G curve of a 1 μm/1 μm medium V_{T0} NMOS transistor is presented. The circle corresponds to

the point which $g_m/I_D = 0.531\,(g_m/I_D)_{max}$.

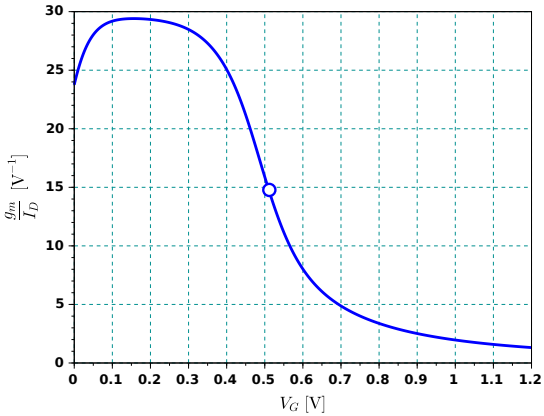

Figure 48: Transconductance-to-current of a medium V_{T0} NMOS vs. gate voltage for $V_{DS} = \phi_t/2$.

Table 12: Simulated parameters of medium V_{T0} NMOS transistor for different aspect ratios.

Parameter	1μm/1μm	1μm/2μm	1μm/5μm	1μm/10μm
V_{T0}	502.7 mV	483.8 mV	469.9 mV	465.1 mV
I_{SQ}	102.6 nA	106.6 nA	109.8 nA	111.5 nA
n	1.314	1.317	1.321	1.326

Table 13: Simulated parameters of medium V_{T0} PMOS transistor for different aspect ratios.

Parameter	1μm/1μm	1μm/2μm	1μm/5μm	1μm/10μm
V_{T0}	467.5 mV	458 mV	452.4 mV	450.8 mV
I_{SQ}	30.2 nA	30.87 nA	31.24 nA	31.54 nA
n	1.421	1.425	1.432	1.438

C.3 TEMPERATURE DEPENDENCE OF THE SPECIFIC CURRENT OF NMOS TRANSISTORS

Using a PTAT drain-to-source voltage source, it was possible to extract the temperature behavior of the specific current for both regular and medium V_{T0} NMOS transistors; the corresponding results are presented in Fig. 49 and Fig. 50. Opposite behavior of the specific currents with the temperature occurs mainly to the differences in the doping concentrations of regular and medium V_{T0} transistors.

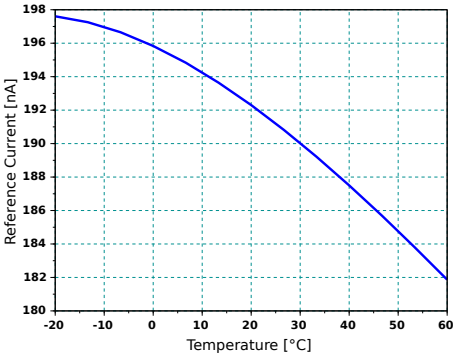

Figure 49: Temperature dependence of the specific current of a regular V_{T0} NMOS transistor.

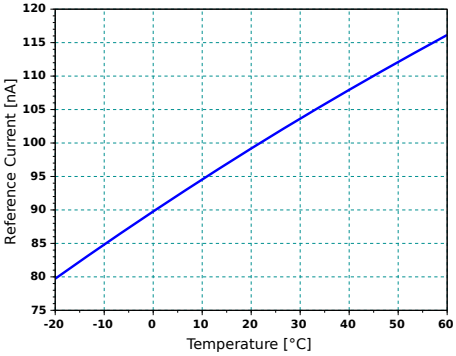

Figure 50: Temperature dependence of the specific current of a medium V_{T0} NMOS transistor.

APPENDIX D – MEASUREMENTS RESULTS OF THE PROOF OF CONCEPT OF THE CURRENT SOURCE

The proof of concept of a CMOS modular current source in GlobalFoundries CMOS 130 nm was designed, using regular V_{T0} transistors in all of the sub-blocks. As was mentioned in Chapter 3 some problems were detected using these transistors. However, this current source was submitted for fabrication, and the laboratory measurements are presented in this appendix.

In this situation, the circuit was designed to generate an output current of 10 nA, with an intermediate voltage $V_{REF} = 2.25\phi_t$. The geometrical ratios used were $\alpha_1 = 9$ and $\alpha_3 = 6$. In this case, the OTA was not implemented with source follower level shifters, thus the deviation in the output current was high, and in only 5 of 40 samples the output current is close to the designed value.

D.1 DC MEASUREMENTS RESULTS

To measure the supply voltage dependence of the current sources, a DC sweep in the V_{DD} from 0 to 1.2 V was performed. The equipment used to measure the output current is the Agilent 4156C Precision Semiconductor Parameter Analyzer, available in the laboratory.

In Fig. 51 the DC measurement results of the 5 samples are presented. In Table 14 the DC measurement results are summarized. Despite the current source is near to the designed value, the line regulation of the output currents is high, probably due to a error in the circuit design.

Table 14: DC measurement results of the output current for the 5 samples.

Sample	I_D	Line Regulation
01	14.5 nA	26.4 %/V
02	10.71 nA	32.7 %/V
03	16.58 nA	14.1 %/V
04	14.82 nA	11.2 %/V
05	16.40 nA	32.5 %/V

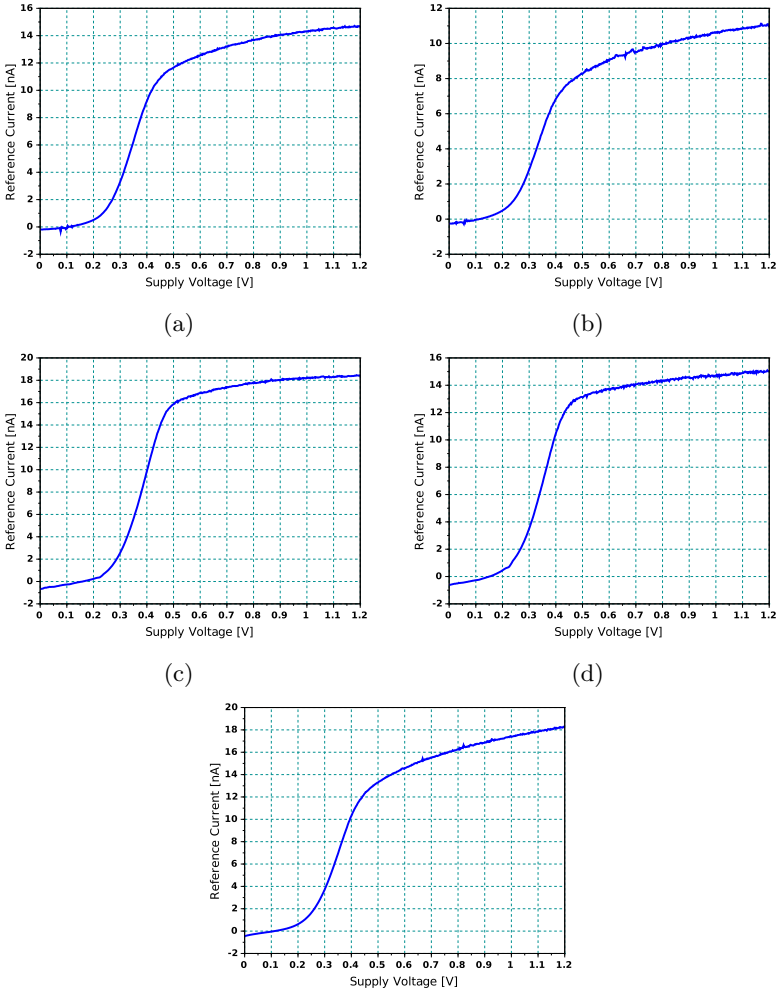

Figure 51: DC measurement results of the output current for the 5 samples.

The temperature dependence of the current source was measured using the Tenney thermal chamber available in the laboratory. The output current measurements were also performed using the 4156C Analyzer. The measurements results are shown in Fig. 52.

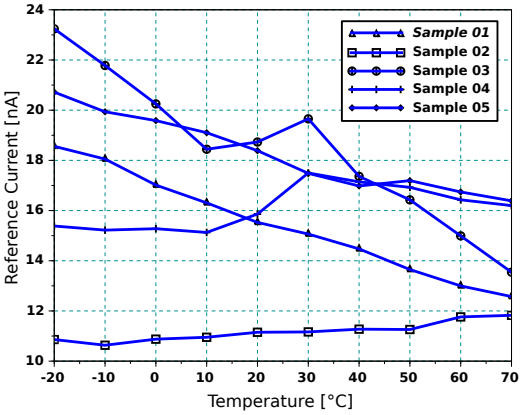

Figure 52: Temperature dependence of the output current for the 5 samples.

As expected, in the most of samples, the output current has a temperature dependence similar to the specific current of the regular V_{T0} transistor presented in Appendix C.